



# SVR ENGINEERING COLLEGE

Approved by AICTE & Permanently Affiliated to JNTUA

Ayyalurmetta, Nandyal – 518503. Website: [www.svrec.ac.in](http://www.svrec.ac.in)

Department of Electronics and Communication Engineering



**DIGITAL COMMUNICATION SYSTEMS LABORATORY**

III B.Tech (ECE) I Semester

2021-2022

STUDENT NAME	
ROLL NUMBER	
SECTION	



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Department of Electronics and Communication Engineering

### DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

#### CERTIFICATE

ACADEMIC YEAR: 2021-2022

*This is to certify that the bonafide record work done by  
Mr./Ms. \_\_\_\_\_ bearing  
H.T.No. \_\_\_\_\_ of III B.Tech I Semester in the **Digital  
Communication Laboratory***

**Faculty In-Charge**

**Head of the Department**

**JAWAHARLALNEHRUTECHNOLOGICALUNIVERSITYANANTAPU  
R**

**B.Tech (ECE) –III-I Sem**

**L**

**TPC**

**0 0 2 1**

**(19A04503P) DIGITALCOMMUNICATIONSLAB**

**Course Objectives**

- To Develops skills for performance analysis of practical digital communication systems.
- To understand the fundamental concepts on TDM, Pulse modulations & digital modulation techniques.
- To evaluate the performance of PCM, DPCM and DM in a digital communication system.
- To learn how to use MATLAB software and hardware effectively and creatively to synthesize digital communication systems.

**LIST OF EXPERIMENTS**

**Minimum of Twelve experiments to be conducted (any six from Part-A) HARDWARE EXPERIMENTS (PART-A)**

1. Generation of random data using linear feedback shift registers at a given data rate. Plot the random data.
2. Construct Time division multiplexing circuit to multiplex three users' data.
3. Verify the functionality of each block in Pulse code modulation system practically.
4. Find the processing gain in a Differential pulse code modulation circuit experimentally.
5. Verify the operation of Delta modulation and demodulation.
6. Design and verify modulated and demodulated circuit for Frequency shift keying.
7. Construct a modulated and demodulated circuit for Differential phase shift keying.
8. Design and verify working principle of QPSK modulation and demodulation with suitable setup.

## SOFTWARE EXPERIMENTS (PART-B)

### Modeling of Digital Communications using MATLAB

1. Study Sampling Theorem and verify the effect of undersampling and oversampling while retrieving the original signal.
2. Understand functioning of each block in Pulse code modulation circuit and verify through simulation.
3. Write a program on Differential pulse code modulation and demodulation.
4. Write a program on Frequency shift keying modulation schemes for given two carrier frequencies, determine the bit error probability.
5. Write a program and verify QPSK modulation and demodulation, determine the bit error probability.
6. Write a program and verify Differential phase shift keying modulation scheme is a non-coherent modulation scheme, determine the bit error probability is inferior to that of QPSK.
7. Write a program and verify QPSK modulation and demodulation, determine the bit error probability.
8. Write a program and verify Differential phase shift keying modulation scheme is a non-coherent modulation scheme, determine the bit error probability is inferior to that of QPSK.

### EQUIPMENT REQUIRED FOR LABORATORIES:

1. RPS - 0-30V
2. CROs - 0-20MHz.
3. Function Generators - 0-1MHz
4. RF Generators - 0-1000MHz.
5. MultiMate's
6. Required Electronic Components (Active and Passive) which include IC's as well.
7. Arbitrary Waveform generators/PNS generators-2Nos. (To generate digital data at required data rates)
8. Licensed MATLAB software with required tool boxes.

### Course Out comes

- Understand real time behavior of different digital modulation schemes and technically visualize spectra of different digital modulation schemes.
- Design and implement different modulation and demodulation techniques.
- Analyze digital modulation & demodulation techniques.
- Simulate all digital modulation and demodulation techniques in MATLAB.

## ECE DEPT VISION & MISSION PEOs and PSOs

### Vision

To produce highly skilled, creative and competitive Electronics and Communication Engineers to meet the emerging needs of the society.

### Mission

- Impart core knowledge and necessary skills in Electronics and Communication Engineering through innovative teaching and learning.
- Inculcate critical thinking, ethics, lifelong learning and creativity needed for industry and society
- Cultivate the students with all-round competencies, for career, higher education and self-employability.

### I. PROGRAMME EDUCATIONAL OBJECTIVES (PEOs)

- PEO1: Graduates apply their knowledge of mathematics and science to identify, analyze and solve problems in the field of Electronics and develop sophisticated communication systems.
- PEO2: Graduates embody a commitment to professional ethics, diversity and social awareness in their professional career.
- PEO3: Graduates exhibit a desire for life-long learning through technical training and professional activities.

### II. PROGRAM SPECIFIC OUTCOMES (PSOs)

- PSO1: Apply the fundamental concepts of electronics and communication engineering to design a variety of components and systems for applications including signal processing, image processing, communication, networking, embedded systems, VLSI and control system
- PSO2: Select and apply cutting-edge engineering hardware and software tools to solve complex Electronics and Communication Engineering problems.

### III. PROGRAMME OUTCOMES (PO'S)

- 1. Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
- 2. Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
- 3. Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

**4. Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

**5. Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

**6. The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

**7. Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

**8. Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

**9. Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

**10. Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

**11. Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

**12. Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

#### **IV. COURSE OBJECTIVES**

- To familiarize the students with basic analog communication systems.
- Integrate theory with experiments so that the students appreciate the knowledge gained from the theory course.
- Understand all types of analog modulation / demodulation principles.
- Substantiate pulse modulation techniques.
- To design and implement different modulation and demodulation techniques.
- To write and execute programs in MATLAB to implement various modulation

Techniques.

**V. COURSE OUTCOMES**

After the completion of the course students will be able to

Course Outcomes	Course Outcome statements	BTL
CO1	Design and conduct experiments, analyze and interpret data of PCM & DPCM	L1
CO2	Design and conduct experiments, analyze and interpret data of DM & TDM	L4
CO3	Design and conduct experiments, analyze and interpret data of FSK, PSK, DPSK & QPSK	L3
CO4	Design different communication applications using digital modulation techniques	L2

**VI. COURSE MAPPING WITH PO'S AND PEO'S**

Course Title	PEO1	PEO2	PEO3	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
DC Lab	3	3	2	3	3	3	3	3	3	3	1	2	2	2	2

**VII MAPPING OF COURSE OUTCOMES WITH PEO'S AND PO'S**

Course Outcomes	PEO1	PEO2	PEO3	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO-1	3	3	2	3	3	3	3	3	3	3	1	2	2	2	2
CO-2	3	3	2	3	3	3	3	3	3	3	1	2	2	2	2
CO-3	3	3	2	3	3	3	3	3	3	3	1	2	2	2	2
CO-4	3	3	2	3	3	3	3	3	3	3	1	2	2	2	2

### **LABORATORY INSTRUCTIONS**

1. While entering the Laboratory, the students should follow the dress code. (Wear shoes and White apron, Female Students should tie their hair back).
2. The students should bring their observation book, record, calculator, necessary stationery items and graph sheets if any for the lab classes without which the students will not be allowed for doing the experiment.
3. All the Equipments and components should be handled with utmost care. Any breakage or damage will be charged.
4. If any damage or breakage is noticed, it should be reported to the concerned in charge immediately.
5. The theoretical calculations and the updated register values should be noted down in the observation book and should be corrected by the lab in-charge on the same day of the laboratory session.
6. Each experiment should be written in the record note book only after getting signature from the lab in-charge in the observation notebook.
7. Record book must be submitted in the successive lab session after completion of experiment.
8. 100% attendance should be maintained for the laboratory classes.

### **Precautions.**

1. Check the connections before giving the supply
2. Observations should be done carefully.



## INDEX

S.NO.	Name of the experiment	Page No.	Performed Date	Date of submission	Marks	Faculty Signature
1						
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## **TIME DIVISION MULTIPLEXING & DEMULTIPLEXING**

### **Introduction:**

Time Division Multiplexing is the technique for simultaneous transmission of more than one intelligence signals on one channel and the single carrier by utilizing the time scale without loss of identity of an individual signal. SS LAB trainer DC-5 (5M & 5D) is a self sustained kit for the demonstration of 2 Channel Time Division Multiplexer & De-multiplexer system. This system provides visual understanding of actual TDM concepts, and this consists of:

### **AIM:**

To Study and verify the process of time division multiplexing & demultiplexing with two different frequency signals.

### **APPARATUS:**

#### **1. TDM Multiplexer:**

1. Regulated power supply.
2. Audio Frequency signal generators.
3. 2 channel TDM multiplexer.
4. Clock generator.
5. Logic source.

#### **2. TDM De-Multiplexer:**

1. Regulated power supply.
2. 2 channel TDM de-multiplexer.
3. Clock generator.
4. 2 no's of passive low pass filters.
5. 2 no's of audio amplifiers.
6. Logic source.

## Block diagram

Figure 1:1 TDM Multiplexer

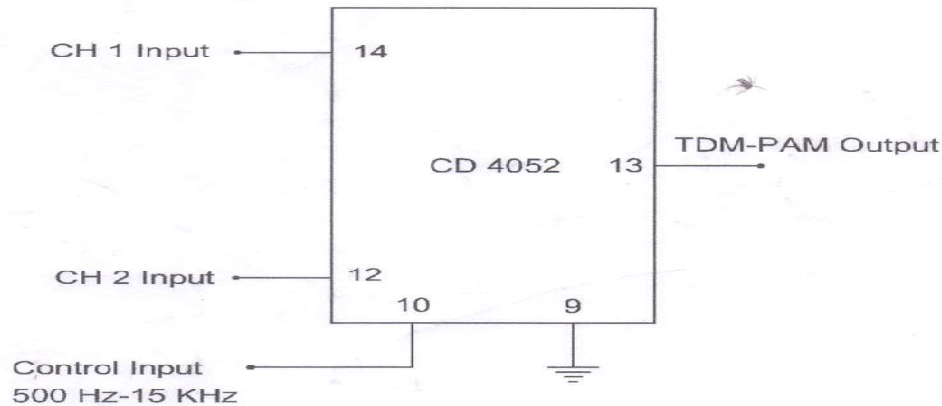
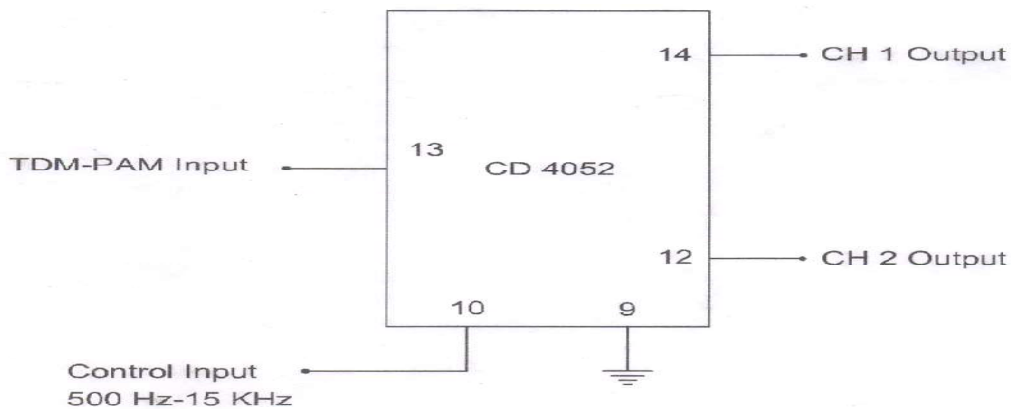


Figure 1:2 TDM De-Multiplexer



### Experimental procedure:

#### Multiplexer:

1. Study the theory of operation.
2. Connect the trainer TDM Multiplexer to the mains and switch on the power supply.
3. Measure the output of the regulated power supply i.e. +5V and -5V with the help of digital millimeter.

4. Observe the output of the AF generator-1 using CRO, it should be a Sine wave of 400 Hz frequency with 3 Vpp amplitude.
5. Observe the output of the AF generator-2 using CRO it should be a Sine wave of 200 Hz frequency with 3 Vpp amplitude.
6. Verify the operation of logic source with multimeter/scope, output should be +5V in logic1 position and 0V in logic 0 position.
7. Observe the output of the Clock generator using CRO; it should be a Square wave of 500 Hz to 15 KHz frequency with 5 Vpp amplitude.
8. Now connect the CH1 & CH2 Inputs of the TDM multiplexer to the outputs of the AF Generator1 and 2 respectively.
9. Connect Control input of the TDM multiplexer to the output of the logic source.
10. Put control signal (logic source) at logic 1 condition and observe the output of the TDM multiplexer with the help oscilloscope, by this we can notice that the output of the TDM multiplexer is a signal which has been connected to CH1 input. In this condition the signal at CH2 input has no effect on multiplexer output.
11. Similarly put logic source at logic 0 position and observe the output of the TDM multiplexer. Now notice that the output of the TDM multiplexer is a signal which has been connected to the CH2 input and the signal at CH1 input has no effect on multiplexer output.
12. Now disconnect logic source and connect clock output to the control input.
13. Observe TDM wave form using CRO at different values of clock frequency, input signal voltage levels and sketch them.

**Note1:** After setting the clock frequency and input signals to desire values put storage scope in STOP mode so that you can view stable display of waveforms.

**Note2:** Sample wave forms given in Figure 1:3, 1:4 are drawn at 1 KHz sampling clock, you can take at any clock frequency.

14. Similarly you can observe and plot the TDM waveforms for different inputs i.e. DC signals alone, AC&DC instead of AC signals.

**Note1:** DC Signals (voltages) can be connected from an external sources and care should be taken in case voltage levels i.e. maximum voltage input voltage must be in range of  $\pm 4.8V$ .

**Note2:** You can use even normal scope, when you observe the TDM wave form for DC inputs.

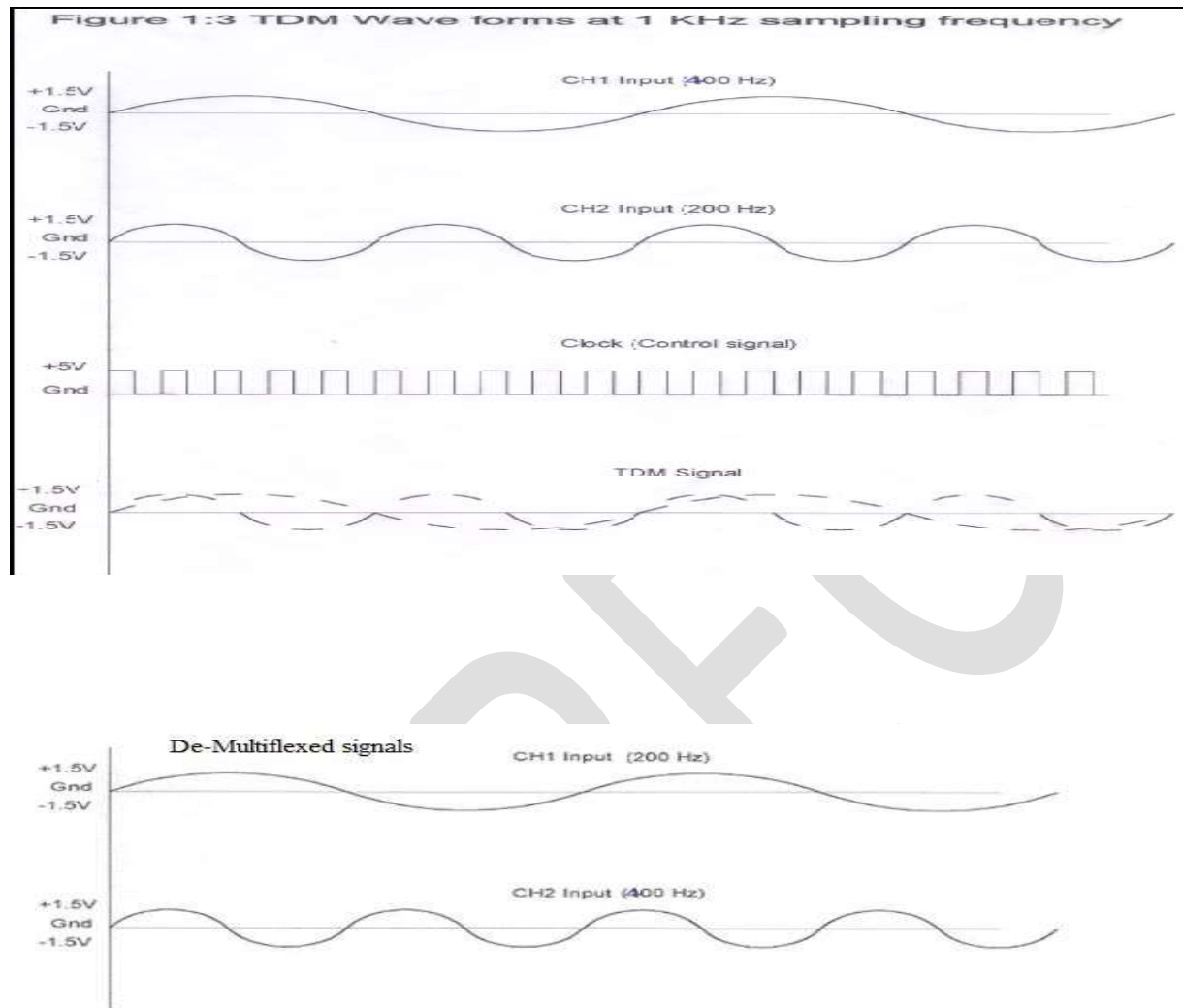
#### **De-multiplexer:**

15. Study the theory of operation.
16. Connect the trainer TDM DE-multiplexer to the mains and switch on the power supply.

17. Measure the output of the regulated power supply i.e. +5V and -5V with the help of digital multimeter.
18. Verify the operation of logic source with multimeter/scope, output should be +5V in logic 1 position and 0V in logic 0 position.
19. Observe the output of the Clock generator using CRO, it should be a Square wave of 500 Hz to 15 KHz frequency with 5 Vp amplitude.
20. Connect TDM-PAM signal to input of TDM de-multiplexer from TDM multiplexer with the help of co-axial cable (supplied with trainer).
21. Connect control input to logic source output.
22. Keep CRO in dual mode; connect one input to CH1 output and another input to CH2 output.
23. Put logic source to 1 position and observe CH1 and CH2 outputs. You can notice that the entire TDM signal is transferred to CH1 output and has no signal at CH2 output.
24. Similarly put logic source to 0 position and observe CH1 and CH2 outputs. Now the entire TDM signal is transferred to CH2 output and has no signal at CH1 output. By the above two steps you can notice that the entire TDM signal is transferred to CH1 output when control input is 1 and to CH2 output when control input is 0.
25. Now disconnect logic source and connect clock from the transmitter (i.e., DC- 5M) through a coaxial cable.
26. Observe CH1 and CH2 outputs. You will notice that the outputs are natural
27. Connect CH1, CH2 outputs to low pass filters and observe the output of the filters and compare them with the original AF Signals ( at multiplexer inputs) using CRO. You will notice that both the signals are same in frequency and shape. Signal amplitude may be attenuated during smoothing process and this can be achieved by taking amplifiers output. Select AC/DC coupling depending on the input signal.

**Observation on effect of synchronization:**

28. Disconnect clock from multiplexer and connect to local oscillator dc-5 with remaining setup as it is. Observe CH1 and CH2 outputs and compare them with the previous results. These signals are little bit distorted in shape. This is because lack of synchronization between clock at multiplexer and clock at de-multiplexer. You can get further perfection in output wave forms by adjusting the locally generated clock.

**EXPECTED WAVE FORMS****Multiplexing:**

Signal	Amplitude	Time Period	Frequency
AF Signal 1			
AF Signal 2			
Clk			
TDM o/p AF <sub>1</sub>			
TDM o/p AF <sub>2</sub>			

**De-multiplexing:**

Signal	Amplitude	Time Period	Frequency
AF Signal 1			
AF Signal 2			

**RESULT:****Viva-Questions:**

1. Define synchronous TDM.
2. Define asynchronous TDM.
3. What is frame in TDM?
4. List out the application of TDM

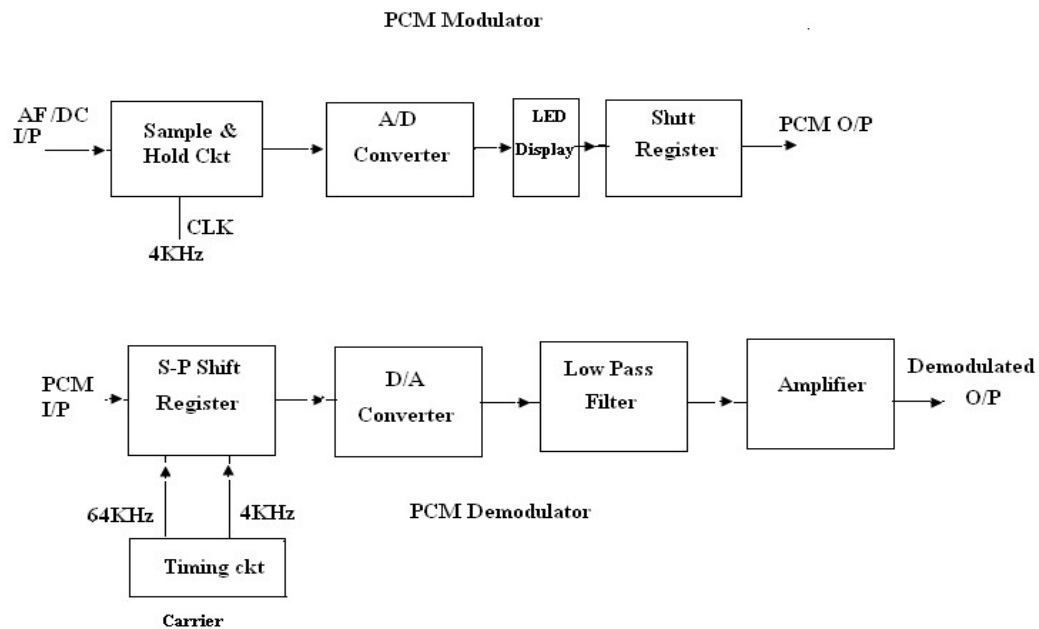
## PULSE CODE MODULATION AND DEMODULATION

**AIM:** To Study & understand the operation of the Pulse code modulation & Demodulation.

**APPARATUS:**

1. PCM Modulator trainer
2. PCM Demodulator trainer
3. Storage Oscilloscope/ Dual Trace Oscilloscope  
(Note: Storage oscilloscope is desired for satisfactory observation of PCM wave forms)
4. Digital multimeter.
5. 2 No.'s of co-axial cables (standard accessories with trainer)
6. patch chords

**CIRCUIT DIAGRAM:**





**THEORY:**

**Pulse modulation:** A form of modulation in which a pulse train is used as the carrier. Information is conveyed by modulating some parameter of the pulses with a set of discrete instantaneous samples of the messages signal. The minimum sampling frequency is the minimum frequency at which the modulating waveform can be sampled to provide the set of discrete values without a significant loss of information.

**PCM:** In pulse code modulation (PCM) only certain discrete values are allowed for the modulating signals. The modulating signal sampled, as in other forms of pulse modulation. But any sample falling within a specified range of values is assigned a discrete value. Each value is assigned a pattern of pulses and the signal transmitted by means of this code. The electronic circuit that produces the coded pulse train from the modulating waveform is termed a coder or encoder. A suitable decoder must be used at the receiver in order to extract the original information from the transmitted pulse train.

**PROCEDURE:**

1. Study the theory of operation thoroughly.
2. Connect the trainer (Modulator) to the mains and switch on the power supply.
3. Observe the output of the AF generator using CRO, it should be a Sine wave of 200Hz frequency with 3Vpp amplitude.
4. Verify the output of the DC source with multimeter / scope, output should vary 0 to +5v.
5. Observe the output of the Clock generator using CRO, they should be 64KHz and 4KHz frequency of square wave with 5 Vp amplitude.

Note: These clock signals are internally connected the circuit so no external connections are required.

6. Connect the trainer (De Modulator) to the mains and switch on the power supply.

7. Observe the output of the clock generator using CRO, it should be 64KHz

Square wave with 5 Vp amplitude.

**PCM Operation (with DC input)****Modulation:**

8. Set DC source to some value say 1 V with the help of multimeter and connect it to the A/D converter input and observe the output LED's.
9. Note down the digital code i.e. output of the A/D converter and compare with the theoretical value  
Theoretical value can be obtained by:

A/D input voltage

$$\text{_____} = X_{(10)} = Y_{(2)}$$

1 LSB value

Where

$$1 \text{ LSB value} = V_{\text{ref}} / 2^n$$

Since  $V_{\text{ref}} = 5\text{V}$  and  $n = 8$

$$1 \text{ LSB Value} = 0.01953$$

**Example:**

A/D input voltage = 1 V

$$= 51.2_{(10)}$$

$$= 00110011_{(2)}$$

So digital output is 00110011

10. Keep CRO in dual mode. Connect one channel to 4KHz signal ( which is connected to the shift register) and another channel to the PCM out put
11. Observe the PCM output with respect to the 4KHz signal and sketch the waveforms. Compare them with the given waveforms

Note: From this wave form you can observe that the LSB bit enters the output first.

**Demodulation:**

12. Connect PCM signal to the demodulators (S-P Shift register) from the PCM modulator (AET-68M) with help of coaxial cable (supplied with the trainer)
13. Connect clock signal (64 KHz) from the transmitter to the receiver using coaxial cable.
14. Connect transmitter clock to the timing circuit
15. Observe and note down the S-P shift register output data and compare it with the transmitted data (i.e output A/D converter at transmitter). You will notice that the output of the S-P shift register is following the A/D converter output in the modulator. Observe D/A converter output (demodulated output) using

multimeter /scope and compare it with the original signal and you can observe that there is no loss in information in process of conversion and transmission.

16. Similarly you can try for different values of modulating signal voltage.

**Sample work sheet:**

- |                             |                              |
|-----------------------------|------------------------------|
| 1. Modulating signal        | : 1V                         |
| 2. A/D output (theoretical) | : 00 11 00 11 <sub>(2)</sub> |
| 3. A/D output (practical)   | : 00 11 00 11 <sub>(2)</sub> |
| 4. S-P output               | : 00 11 00 11 <sub>(2)</sub> |
| 5. D/A Converter output     | : 1V (Demodulation output)   |

**PCM Operation (with AC input)**

**Modulation:**

17. Connect AC signal of  $2V_{pp}$  amplitude to Sample & Hold circuit.
18. Keep the CRO in dual mode. Connect one channel to the AF signal and another channel to the sample & hold output. Observe and sketch the sample & hold output.
19. Connect the sample and hold output to the A/D converter and observe the PCM output using storage oscilloscope/ DTO
20. Observe PCM output by varying AF signal voltage.

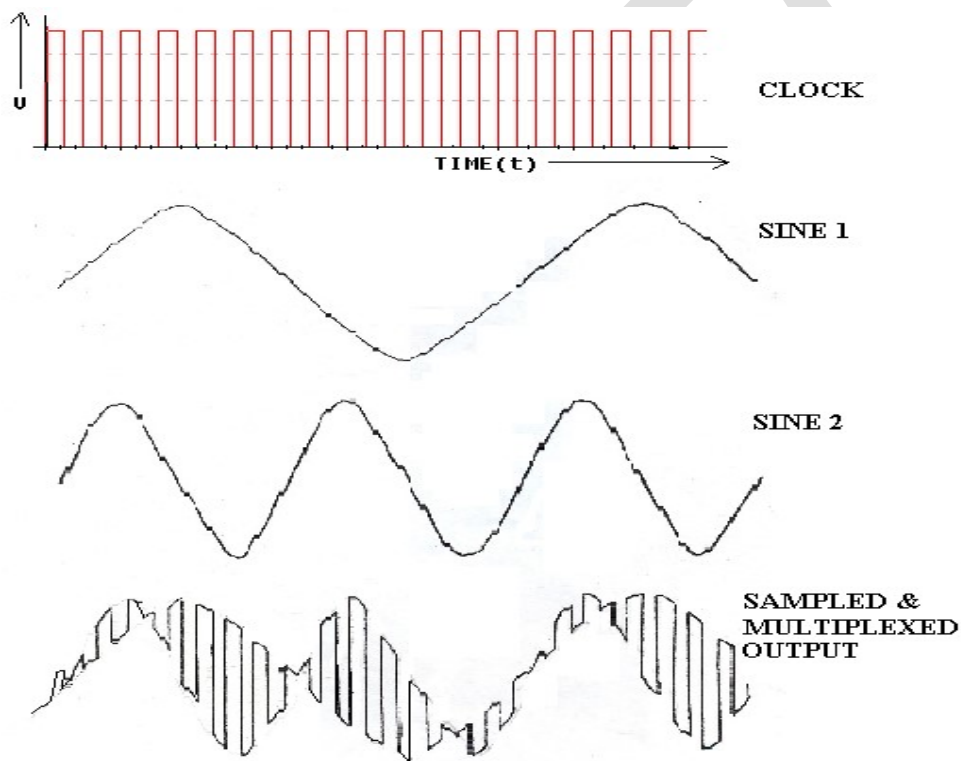
**DEMODULATION**

21. Connect PCM signal to the demodulator input (S-P shift register) from the PCM modulator with the help of coaxial cable (supplied with the trainer)
22. Connect clock signal (64KHz) from the transmitter to the receiver using coaxial cable
23. Connect transmitter clock to the timing circuit.
24. Keep CRO in dual mode. Connect CH 1 input to the sample and hold output and CH 2 input of the D/A converter output .
25. Observe and sketch the D/A output.
26. Connect D/A output to the LPF input.
27. Observe output of the LPF/Amplifier and compare it with the original modulating signal .
28. From above observation you can verify that there is no loss in information (modulating signal) in conversion and transmission process.

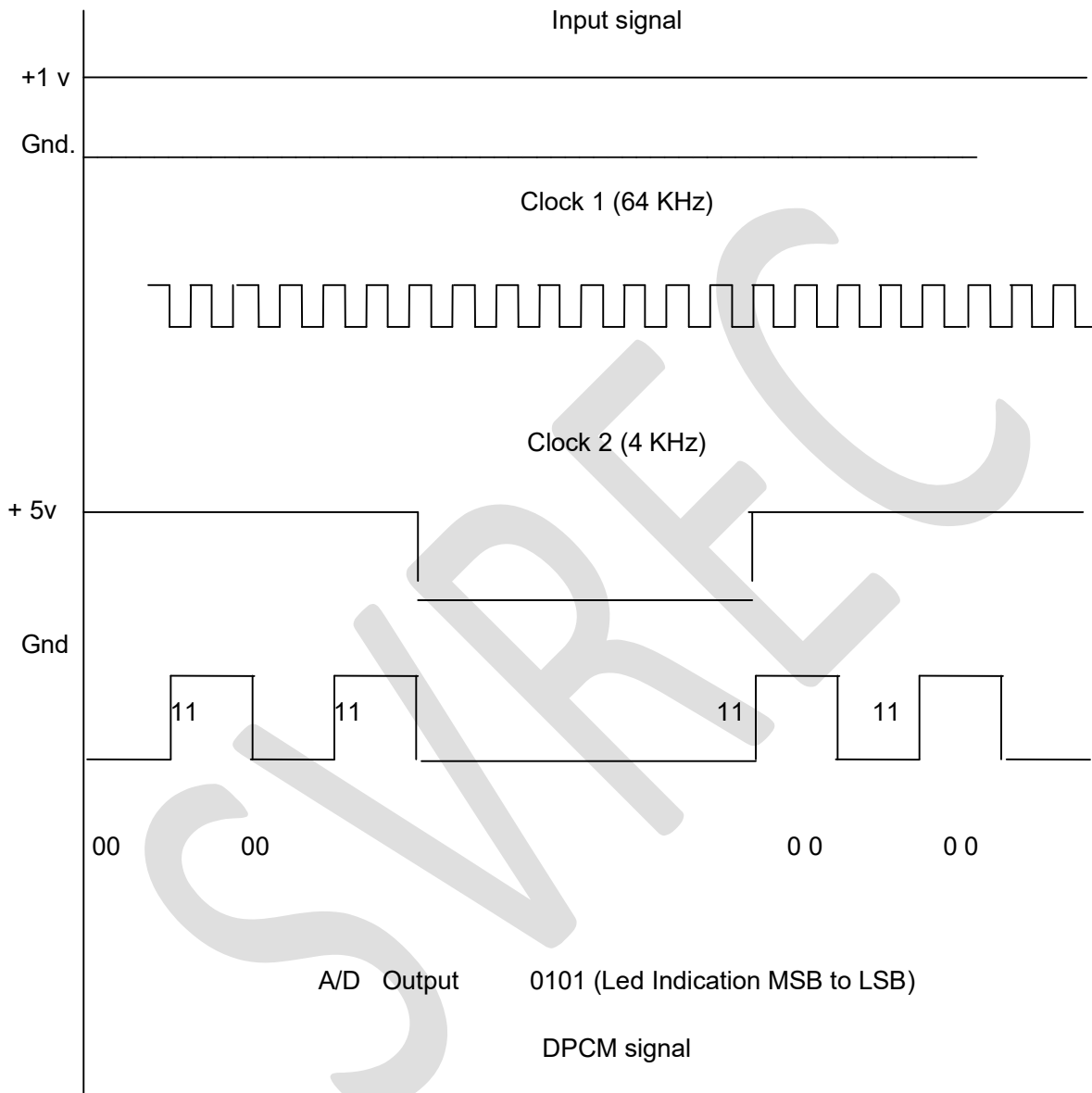
29. Disconnect clock from transmitter and connect to local oscillator (i.e. clock generator output from De Modulator) with remaining setup as it is. Observe D/A output and compare it with the previous result. This signal is little bit distorted in shape. This is because lack of synchronization between clock at transmitter and clock at receiver.

Note: You can take modulating signals from external sources. Maximum amplitude should not exceed 4V in case of DC and 3V<sub>pp</sub> in case of AC (AF) signals.

### EXPECTED WAVEFORMS:

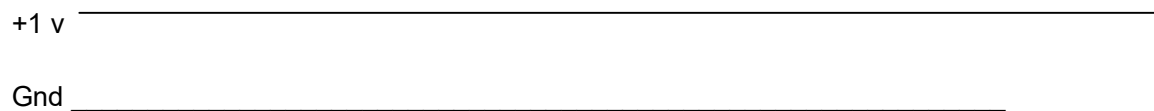


PCM wave forms/ timing diagram of DC input



S – P : Register output 0101 (Led Indication MSB to LSB)

D/A output (demodulated signal)



**Samplework sheet:**

1. Modulating signal :4.4V
2. A/D Output(theoretical) :11100001(2)
3. A/D Output (practical) : 1110  
0001(2)
4. S-P Output :11100001(2)
5. D/A Converter output : 4.4  
V(Demodulated output)

**OBSERVATIONS:**

Sampled value 1: V                      PCM output: (8bit binary)

Signal	Amplitude	Time Period	Frequency
D.C input Signal			
Input signal			
Clock1			
Clock2			
Demodulated Output			

**RESULT:****QUESTIONS:**

1. Differentiate PCM over Analog modulation?
2. What is bit synchronization & frame synchronization?
3. Explain block diagram of PCM?
4. What is the different error control coding technique?
5. What is resolution in ADC?

## **DELTA MODULATION & DEMODULATION**

**Aim:** To Study the operation of Delta modulation and demodulation technique.

### **Equipment required:**

1. DM Modulator trainer
2. DM Demodulator trainer
3. Storage Oscilloscope  
(Note: Storage oscilloscope is desired for satisfactory observation of DM wave forms)
4. Digital multimeter.
5. 2 No's co-axial cables (standard accessories with trainer)

**DM:** Delta modulation is almost similar to differential PCM. In this, only one bit is transmitted per sample just to indicate whether the present sample is larger or smaller than the previous one. The encoding, decoding and quantizing process become extremely simple but this system cannot handle rapidly varying samples. This increases quantizing noise. It has also not found wide acceptance.

Delta Modulation & Demodulation is a self sustained and well organized kit for the demonstration of delta modulation & demodulation. Basic circuits those are well known to every electronic student have been used in this trainer system. And this is absolute practical implementation of delta modulation theory which we come across in class room. This unique system consists of:

### **DM Modulator:**

1. Regulated power supply.
1. Audio Frequency signal generator.
2. Buffer/Signal shaping network.
3. Voltage comparator.
4. 4 Bit UP/DOWN Counter.
5. Clock generator/ Timing circuit.

### **DM Demodulator:**

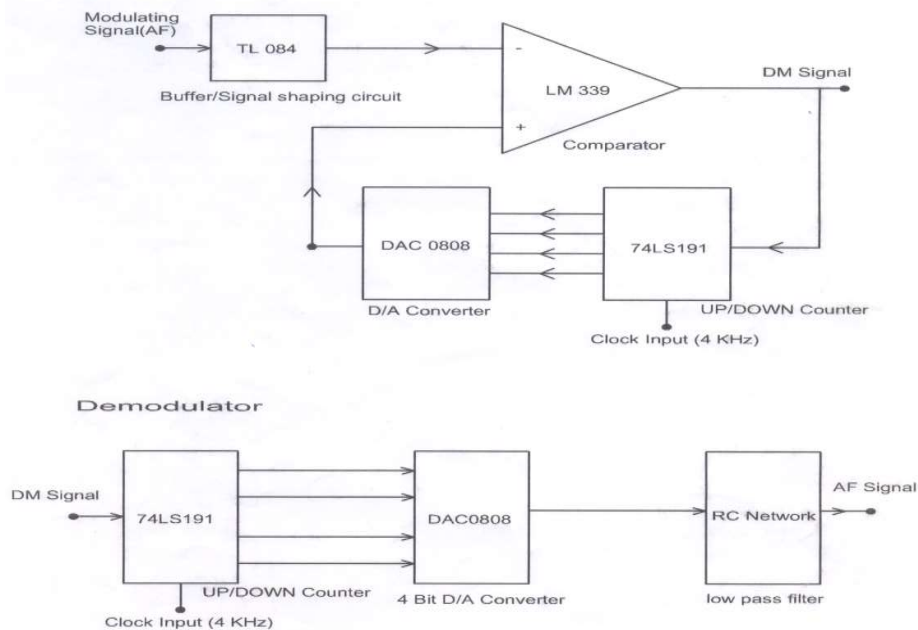
7. Regulated power supply.
8. 4 Bit UP/DOWN Counter.
9. 4 Bit D/A converter.
10. Clock generator.
5. Passive low pass filter , audio amplifier

### Block diagram/Circuit description:

#### Regulated power supply :

This consists of a bridge rectifier followed by Capacitor filters and three terminal regulators 7805 and 7905 to provide regulated DC voltages of  $\pm 5V$  and  $+12V @ 300 mA$  each to the on board circuits. These supplies have been *internally connected to the circuits*, so no external connections are required for operation.

Figure 1:1 DM System Modulator



#### **DM Operation:**

Figure 1:1 shows the basic block diagram of the PCM system. The modulating signal is applied to buffer/signal shaping network. This applied signal will be super imposed by  $+1.5V$  DC so that the negative portion the modulating signal will clamped to positive, this process is needed, because input of the comparator should be between 0 and  $+3V$ .



After level shifting is done the signal will be passed to inverting input of the comparator. Non inverting input of the comparator is connected to output of the 4 Bit D/A converter. Comparator is operating at +5V single supply. So output of the comparator will be high (i.e +veV<sub>sat</sub>) when modulating signal is less than the reference signal i.e. D/A output, other wise it will be 0 V. And this signal is transmitted as Delta Modulation signal. Same signal is also connected as UP/DOWN control to the UP/DOWN counter (74ls191).

UP/DOWN counter is programmed for 0000 starting count. So initially (i.e. when we switch on power supply) out put of the counter is at 0000 and the D/A converter will be at 0V. Comparator compares the modulating signal and reference signal (D/A Output). Comparator output will be 0 if the modulating signal is greater than the reference signal. For next clock pulse depending on the UP/DOWN input (i.e. DM signal) counter will count up or down. If the UP/DOWN input is low (nothing but comparator output), counter will make up and output will be 0001. So the D/A converter will convert this 0001 digital input to equivalent analog signal (i.e. 0.3V 1 LSB Value). Now the reference signal is 0.3V, If still modulating signal is greater than the D/A output again comparator output (DM) will be low and UP count will occur. If not DOWN count will take place. This process will continue till the reference signal and modulating signal voltages are equal. So DM signal is a series of 1 and 0.

DM signal is applied to a UP/DOWN input of the UP/DOWN counter at the receiver. This UP/DOWN counter is programmed for 1001 initial value (i.e. power on reset) and mode control is activated. So depend on the UP/DOWN input (DM Signal) for the next

clock pulse counter will count UP or DOWN. This output is applied to 4 Bit D/A converter. A logic circuit is added to the counter which keeps the output of the counter in between 0000 and 1111 always. Output of the D/A converter will be a staircase signal lies between 0 and

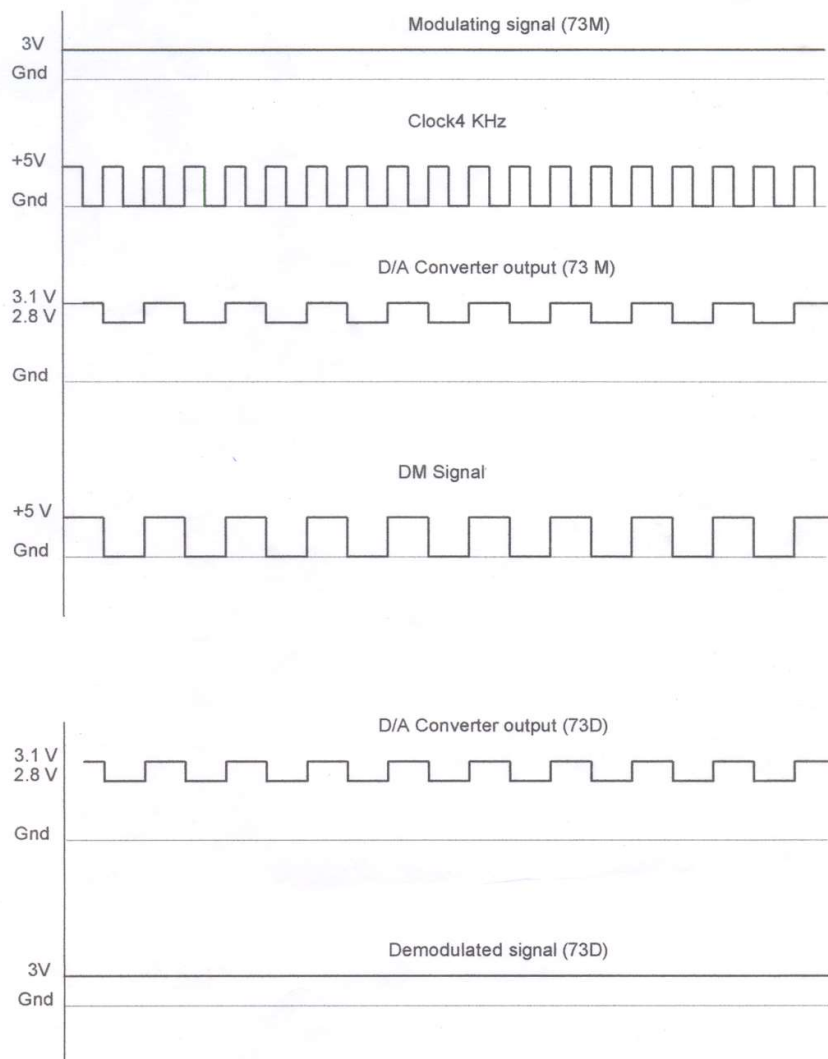
+4.7V. This stair case signal is applied a low pass filter. This low pass will smoothen the staircase signal so that original AF signal will be recovered.

We can use a voltage amplifier at the output of the low pass filter to amplify the recovered AF signal to desired voltage level.

**Experimental procedure:****DM Modulator:**

29. Study the theory of operation.
2. Connect the trainer (DM Modulator) to the mains and switch on the power supply.
3. Observe the output of the AF generator using CRO, it should be a Sine wave of 100 Hz frequency with 3Vpp amplitude.
4. Verify the output of the DC source with multimeter/scope; output should vary 0 to +4v.
5. Observe the output of the Clock generator using CRO, they should be 4 KHz frequency of square wave with 5 Vpp amplitude.
- 6 Note: This clock signal is *internally connected to the up/down counter* so no external connection is required

Figure 1:2 DM Wave forms/Timing diagrams (3 V DC Input).



**DM With DC Voltage as modulating signal:**

1. Connect dc signal from the DC source to the inverting input of the comparator and set some voltage say 3V.
2. Observe and plot the signals at D/A converter output (i.e., non-inverting input of the comparator), DM signal using CRO and compare them with the wave forms given in figure 1:2.
3. Connect DM signal (from Modulator) to the DM input of the demodulator.
  
30. Connect clock (4 KHz) from modulator to the clock input of the demodulator. Connect clock input of the UP/DOWN counter to the clock from transmitter with the help of springs provided.
31. Observe digital output (LED Indication) of the UP/DOWN counter and compare it with the output of the UP/DOWN. By this you can notice that the both the outputs are same.
32. Observe and plot the output of the D/A converter and compare it with the wave forms given in Figure 1:2.
33. Measure the demodulated signal (i.e. output of the D/A converter with the help of multimeter and compare it with the original signal.
34. From above observation you can notice that the both the voltages are equal and there is no loss in process of modulation, transmission and demodulation.
35. Similarly you can verify the DM operation for different values of modulating signal.

**DM With AF signal as modulating signal:**

36. Connect AF signal from AF generator to the inverting input of the comparator and set output amplitude at 3Vpp.
37. Observe and plot the signals at D/A converter output (i.e., non-inverting input of the comparator), DM signal using CRO and compare them with the wave forms given in figure 1:3.
38. Connect DM signal to the DM input of the demodulator.
39. Connect clock (4 KHz) from modulator to the clock input of the demodulator. Connect clock input of the UP/DOWN counter to the clock from transmitter with the help of springs provided.
40. Observe and plot the output of the D/A converter and compare it with the wave forms given in Figure 1:3.
41. Observe and sketch the D/A output.
42. Connect D/A output to the LPF input.
43. Observe the output of the LPF/Amplifier and compare it with the original modulating signal.
  
44. From above observation you can verify that there is no loss in information (modulating signal) in conversion and transmission process. Disconnect clock from transmitter and connect to local oscillator (i.e., clock generator output from with remaining setup as it is. Observe demodulated signal output and compare it with the previous result. This signal is little bit distorted in shape. This is because lack of synchronization between clock at transmitter and clock at receiver.

**Note:** you can take modulating signals from external sources. Maximum amplitude should not exceed 4 V in case of DC and 3 Vpp in case of AC (AF) signals.

Figure 1:3 DM Wave forms/Timing diagrams (Modulation) (3Vpp AFInput).

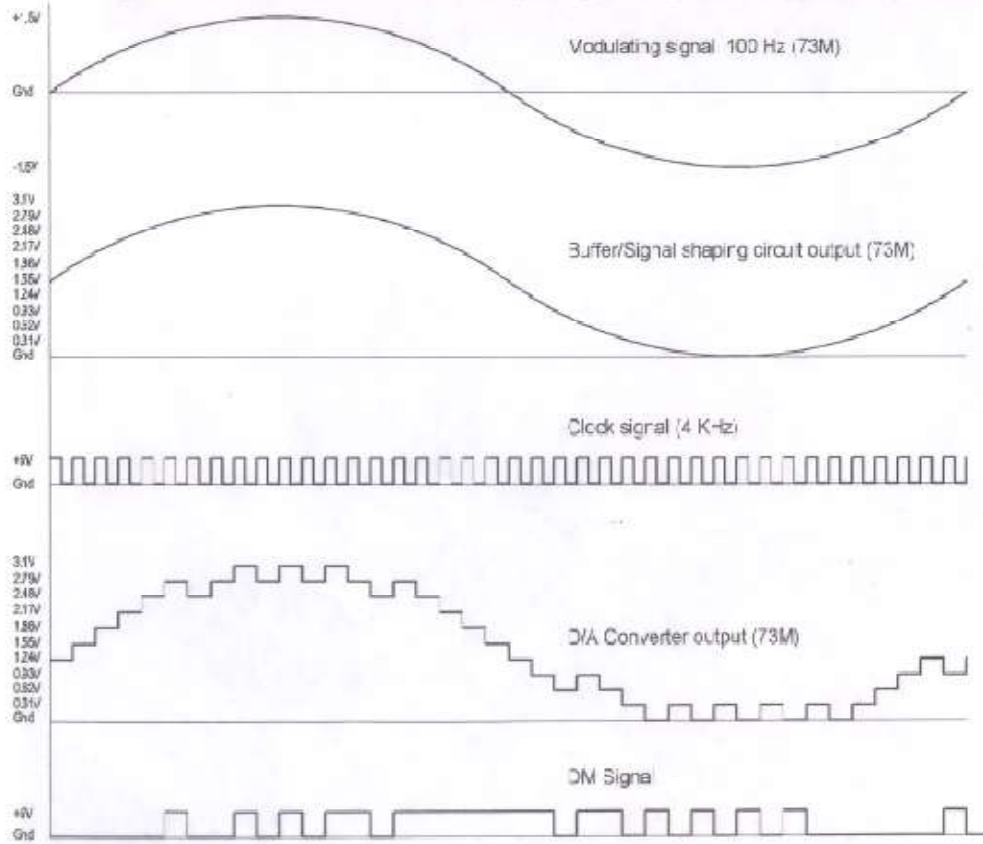
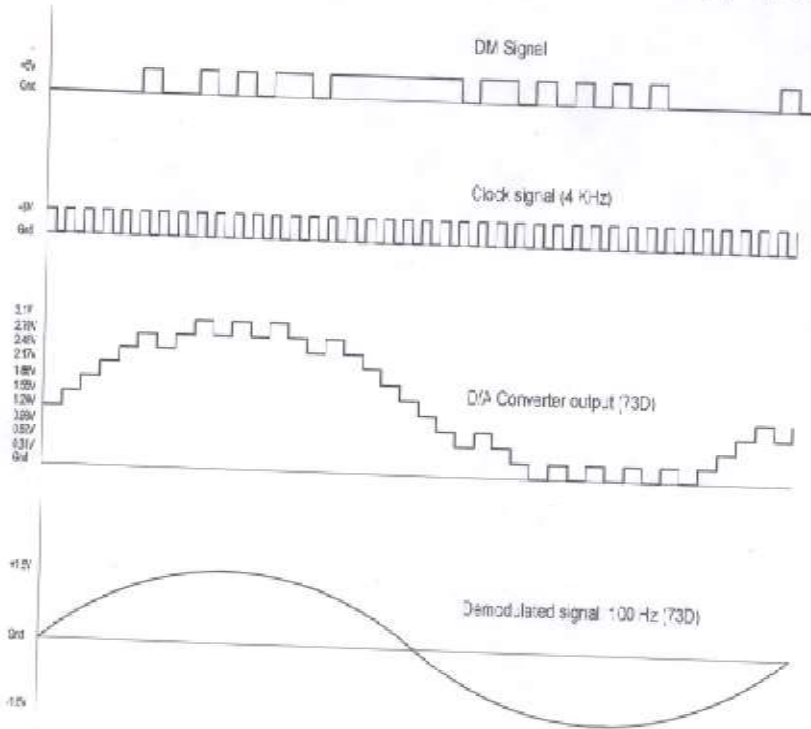


Figure 1:3 DM Wave forms/Timing diagrams (Demodulation) (3Vpp AFInput).



**Observation table:-**

Signal	Amplitude	Time Period	Frequency
AF Signal			
Transmitter Clk			
Demodulated signal			

Delta Modulation output:

(Binary values)

**RESULT:**

**Viva Questions:**

1. How analog signal can be coded into bits?
2. What is the advantage of DM over PCM?
3. Which types of noise occur in delta modulation?
4. Define adaptive delta modulation

## **FREQUENCY SHIFT KEYING**

**AIM:** Study the operation of FSK modulation & Demodulation and to plot the FSK wave forms for Binary data at different frequencies.

### **Theory:**

Frequency Shift Keying(FSK) is a modulation/ Data transmitting technique in which carrier frequency is shifted between two distinct fixed frequencies to represent logic 1 and logic 0. The low carrier frequency represents a digital 0(Space) and higher carrier frequency is a

1 (mark). FSK system has a wide range of application in low speed digital data transmission systems. Wave forms are shown in figure 1:3.FSK Modulating & Demodulating circuitry can be developed in number of ways, familiar VCO and PLL circuits are used in this trainer. Figure1:1 and figure 1:2 shows the FSK modulator and demodulator respectively.

### **Equipment required:**

1. Frequency shift keying system trainer
2. Dual trace Oscilloscope
3. Digital Multimeter
4. Digital Frequency Counter

### **FSK Modulator:**

Figure 1:1 shows the FSK modulator using IC XR 2206.ICXR 2206 is a VCO based monolithic function generator capable of producing Sine, Square, Triangle signals with AM and FM facility. In this trainer XR2206 is used generate FSK signal. Mark(Logic 1) and space (logic 0) frequencies can be independently adjusted by the choice of timing potentiometers F0& F1. The output is phase continuous during transitions. The keying signal I.E. data signal is applied to Pin9.

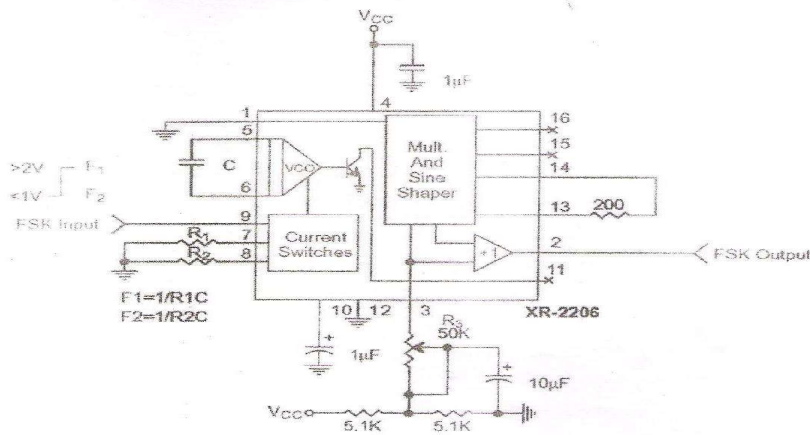
**Figure1:1 FSK Modulator Using XR2206****FSK Demodulator:**

Figure 1:2 Shows FSK Demodulator, is a combination of PLL (LM565) and comparator (OP-amp). The frequency-Changing signal at the input to the PLL drives the phase detector to result in rapid change in the error voltage, which is applied to the input of the comparator. At the space frequency, the error voltage out of the phase detector is below the comparison voltage of the comparator. The comparator is a non-inverting circuit, so its output level is also low. As the phase detector input frequency shifts low (to the mark frequency), the error voltage steps to a high level, passing through the comparison level, causing the comparator output voltage to go high. This error voltage change will snap the comparator output voltage between its two output levels in manner that duplicates the data signal input to the XR2206 modulator.

The free running frequency of the PLL (no input signal) is set midway between the mark and frequencies .A space frequencies. A Space at 2025 Hz and mark at 2225 Hz will have a free running VCO Frequency of 2125Hz.



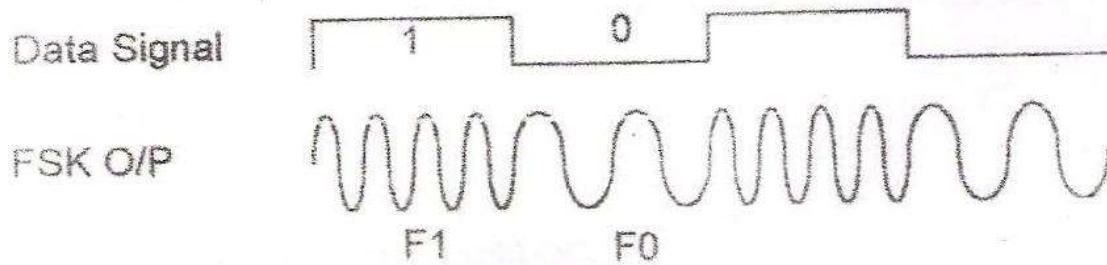
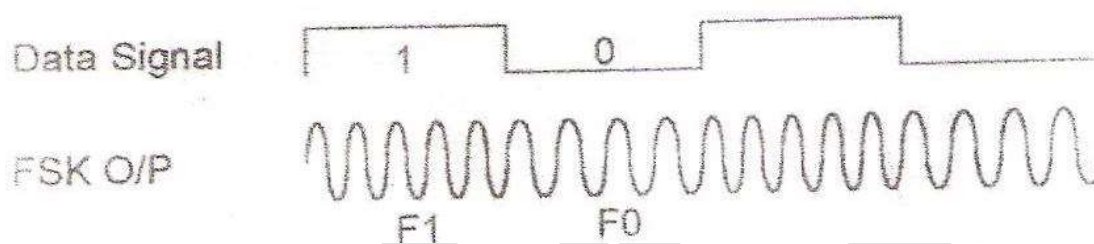


13. Keep CRO in dual mode connect CH1 input of the oscilloscope to the input of the FSK modulator and CH2 input to the output of the FSK modulator.
14. Observe the FSK signal for different data signal frequencies and plot them. By this we can observe that the carrier frequency is shifting between two signals is 0 and 2.4 KHZ when data signal is 0 and 2.4 KHZ when data input is 1 in this case.
15. Compare those plotted wave forms with the theoretically drawn in figure 1:3.

### **FSK Demodulation:**

16. Again connect input of the FSK modulator to the logic source and put data source switch in 0 positions.
17. Connect the frequency counter to the output of the FSK modulator output.
18. Set FSK output frequency to 2025 Hz with the help of F) control.
19. Now put data source switch in 1 position and set the FSK output frequency to 2225 Hz with the help of F1 control without disturbing the F0.  
**NOTE:** As per one of the standards, for proper demodulation of FSK signal the F0 the data signal generator.
20. Disconnect the FSK input of the modulator from logic source and connect to the data signal generator.
21. Observe the output of the modulator using CRO and compare them with given waveforms in figure 1:3.
22. Now connect the FSK modulator output to the FSK input of the demodulator.
23. Connect CH1 input of the Oscilloscope to the data signal at modulator and CH2 input to the output of the FSK demodulator (Keep CRO in dual Mode).
24. Observe and plot the output of the FSK demodulator for different frequencies of data signal. Compare the original data signal and demodulated signal; by this

We can observe that there is no loss in process of FSK modulation and demodulation.

FSK Wave form for  $F_0$  (1.2 KHz ) and  $F_1$  ( 2.4 KHz )FSK Wave form for  $F_0$  (2025 Hz ) and  $F_1$  ( 2225 Hz )**OBSERVATIONTABLE:**

Signal	Amplitude	Frequency
Data signal		
Carrier1		
Carrier2		
Data at receiver o/p		

FrequencyofFSKoutputofLogic1:

FrequencyofFSKoutputofLogic0:

**RESULT:****VIVA-QUESTIONS:**

1. Why FSK is preferred over ASK?
2. What is BFSK?
3. What is the difference between FM and FSK?
4. What is the bandwidth of BFSK?
5. What is the disadvantage of BFSK?

## DIFFERENTIAL PULSE CODE MODULATION AND DEMODULATION

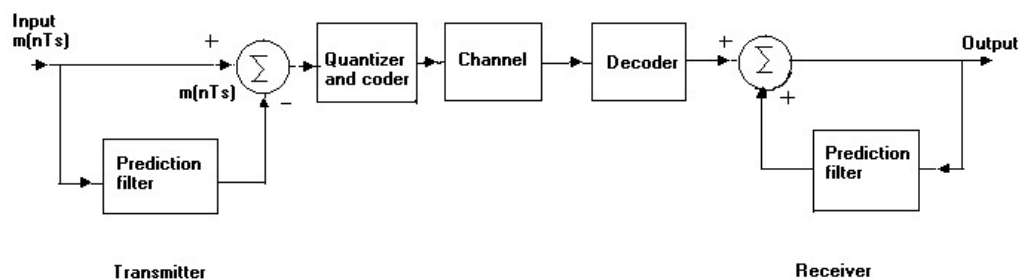
**AIM:** To Study & understand the operation of the DPCM

**APPARATUS:**

7. DPCM Modulator trainer
8. DPCM Demodulator trainer
9. Storage Oscilloscope
10. Digital Multimeter.
11. 2 No's of co- axial cables (standard accessories with trainer)
12. Patch chords
- 13.

**BLOCK DIAGRAM:**

Block diagram of DPCM



**THEORY:**

Differential PCM is quite similar to ordinary PCM. However, each word in this system indicates the difference in amplitude, positive or negative, between this sample and the previous sample. Thus the relative value of each sample is indicated rather than, the absolute value as in normal PCM.

This unique system consists of

**I. DPCM Modulator**

1. Regulated power supply
2. Audio Frequency signal generator
3. Prediction Filter
4. Sample & Hold circuit

5. A/D Converter
6. Parallel –Serial Shift register
7. Clock generator / Timing circuit
8. DC source

## II. DPCM Demodulator

1. Regulated Power Supply
2. Serial-Parallel Shift registers.
3. D/A converter.
4. Clock generator
5. Timing circuit
6. Prediction filter
7. Passive low pass filter

### **PROCEDURE:**

6. Study the theory of operation thoroughly.
7. Connect the trainer (Modulator) to the mains and switch on the power supply.
8. Observe the output of the AF generator using CRO, it should be Sine wave of 400 Hz frequency with 3V pp amplitude.
9. Verify the output of the DC source with millimeter/scope; output should vary 0 to +290mV.
10. Observe the output of the Clock generator using CRO, they should be 64 KHz and 8 KHz frequency of square with 5 Vpp amplitude.
11. Connect the trainer (De Modulator) to the mains and switch on the power supply.
12. Observe the output of the Clock generator using CRO ; it should be 64KHz square wave with amplitude of 5 pp.

### **DPCM Operation (with DC input):**

#### **Modulation:**

13. Keep CRO in dual mode. Connect one channel to 8 KHz signal (one which is Connected to the Shift register) and another channel to the DPCM output.
14. Observe the DPCM output with respect to the 8 KHz signal and sketch the Waveforms.

Note: Form this waveform you can observe that the LSB bit enters the output

First.

#### **Demodulation:**

15. Connect DPCM signal to the demodulator (S-P register) from the DPCM modulator with the help of coaxial cable (supplied with the trainer).
16. Connect clock signal (64KHz) from the transmitter to the receiver using coaxial cable.
17. Connect transmitter clock to the timing circuit.
18. Observe and note down the S-P shift register output data and compare it with the transmitted data (i.e output A/D converter at transmitter) notice that the output of the S-P shift register is following the A/D converter output in the modulator.
19. Observe D/A converter output (demodulated output) using multimeter/scope and compare it with the original signal and can observe that there is no loss in information in process of conversion and transmission.

### **DPCM Operation (with AC input):**

#### **Modulation:**

20. Connect AC signal of  $3V_{PP}$  amplitude to positive terminal of the summer circuit.  
Note: The output of the prediction filter is connected to the negative terminal of the summer circuit and can observe the waveforms at the test points provided on the board.
21. The output of the summer is internally connected to the sample and hold circuit
22. Keep CRO in dual mode. Connect one channel to the AF signal and another channel to the Sample and Hold output. Observe and sketch the sample & hold output
23. Connect the Sample and Hold output to the A/D converter and observe the DPCM output using oscilloscope.
24. Observe DPCM output by varying AF signal voltage.

#### **Demodulation:**

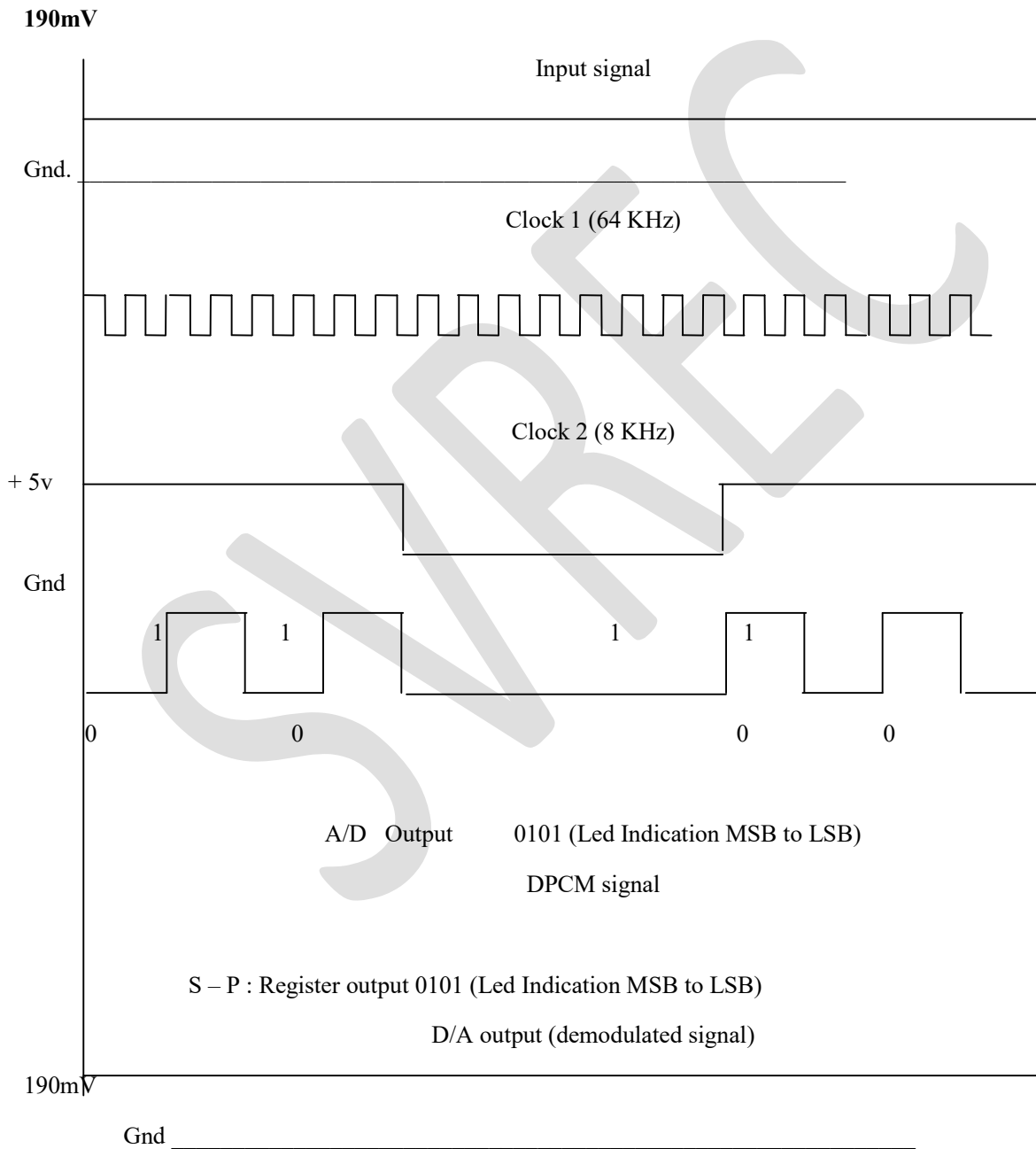
25. Connect DPCM signal to the demodulator input (S-P shift register) from the DPCM modulator with the help of coaxial cable (supplied with trainer).
26. Connect clock signal (64KHz) from the transmitter to the receiver using coaxial cable.
27. Connect transmitter clock to the timing circuit.
28. Keep CRO in dual mode. Connect one channel to the sample & hold output and another channel to the D/A converter output ..
29. Observe and sketch the D/A output
30. Connect D/A output to the LPF input and observe the output of the LPF.
31. Observe the wave form at the output of the summer circuit.
32. Disconnect clock from transmitter and connect to the local oscillator(i.e., clock generator output from De Modulator) with remaining setup as it is. Observe D/A output and compare it with the

previous result. This signal is little bit distorted in shape. This is because lack of synchronization between clock at transmitter and clock at receiver.

**EXPECTED WAVEFORMS:**

Draw the wave forms for the given DC input (190mV) corresponding binary data wave form, and for AC input draw sample and hold waveform then D/A converter o/p and then reconstructed AC signal

**DPCM way form / timing diagram DC input**



**TABLE 1**

Example for complete DPSK operation (with arbitrary bits 0)

Message signal (to be transmitted)	0	1	1	0	0	
Encoded data (differential data)	0	1	1	1	0	1
Transmitted signal phase	180	0	0	0	180	0
Received signal phase	180	0	0	0	180	0
Message signal (demodulated)		0	1	1	0	0

**OBSERVATIONS: DPCM with AC input**

	Amplitude	Time period
AC Input		
Prediction Filter Output		
Sample and Hold Output		
Clock -1 output		
DPCM Output		

**Demodulation:**

	Amplitude	Time period
DPCM Input		
D/A Converter Output		
LPF Output		
Demodulation Output		
Prediction Filter output		

**RESULT:****VIVA QUESTIONS:-**

- 1 What is PSK?
- 2 What is the disadvantage of PSK?
- 3 What is BPSK?
- 4 How BPSK is generated?
- 5 What is the advantage of PSK?

## QPSK GENERATION AND DETECTION

**AIM:** To study modulation and demodulation of QPSK and sketch the relevant waveforms.

### APPARATUS:

1. QPSK Trainer Kit
2. Dual Trace oscilloscope
3. Digital Millimeter
4. C.R.O(30MHz)
5. Patch chords.

### THEORY:

The Quadrature Phase Shift Keying QPSK is a variation of BPSK, and it is also a Double Side Band Suppressed Carrier DSBSC modulation scheme, which sends two bits of digital information at a time, called as bigits. Instead of the conversion of digital bits into a series of digital stream, it converts them into bit pairs. This decreases the data bit rate to half, which allows space for the other users

### BLOCK DIAGRAM: QPSK MODULATOR & DEMODULATOR

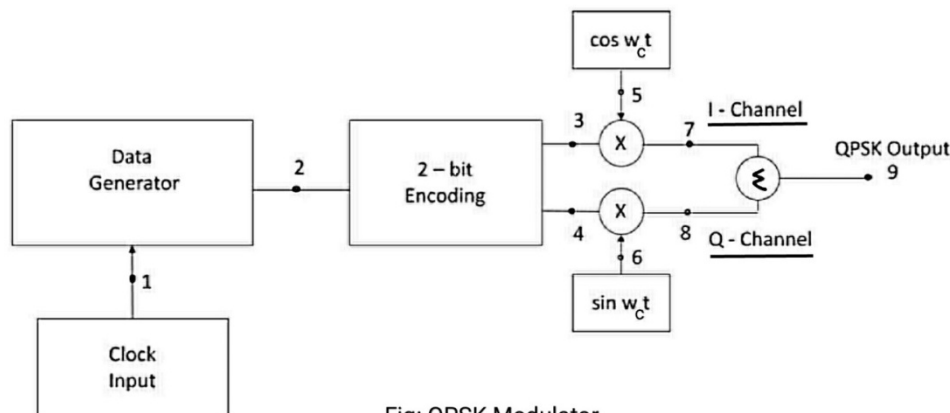


Fig: QPSK Modulator

### PROCEDURE:

1. Connect and switch on the power supply.
2. QPSK is selected by default and LEDs of corresponding technique will glow.
3. Select the bit pattern using push button i.e. 8 bit or 16 bit or 32 bit or 64 bit. Observe bit pattern on TP-2.
4. Select data rate using push button i.e. 2 KHz or 4 KHz or 8 KHz 16 KHz.

### Modulation:

5. Observe the input bit pattern at TP-2 by varying bit pattern using respective pushbutton.
6. Observe the data rate at TP-1 by varying data rate using respective pushbutton.
7. Observe the Two-bit encoding i.e. I-Channel (TP-3) and Q-Channel (TP-4).
8. Observe carrier signal i.e. cosine wave (TP-5) and sine wave (TP-6). Frequency of carrier signal will change with respect to data rate.



9. Observe I-Channel (TP-7) and Q-Channel (TP-8) modulated signal.

10. Observe QPSK modulated signal at TP-9.

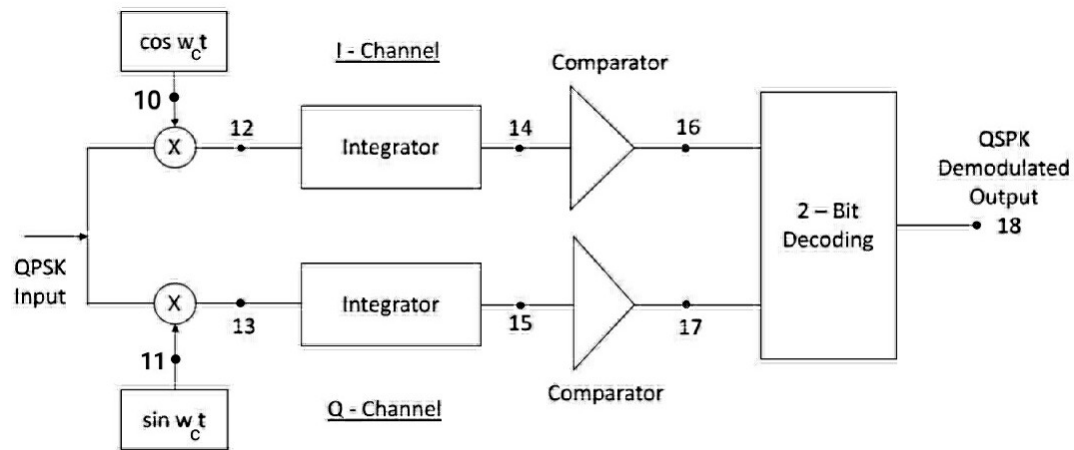


Fig: QPSK Demodulator

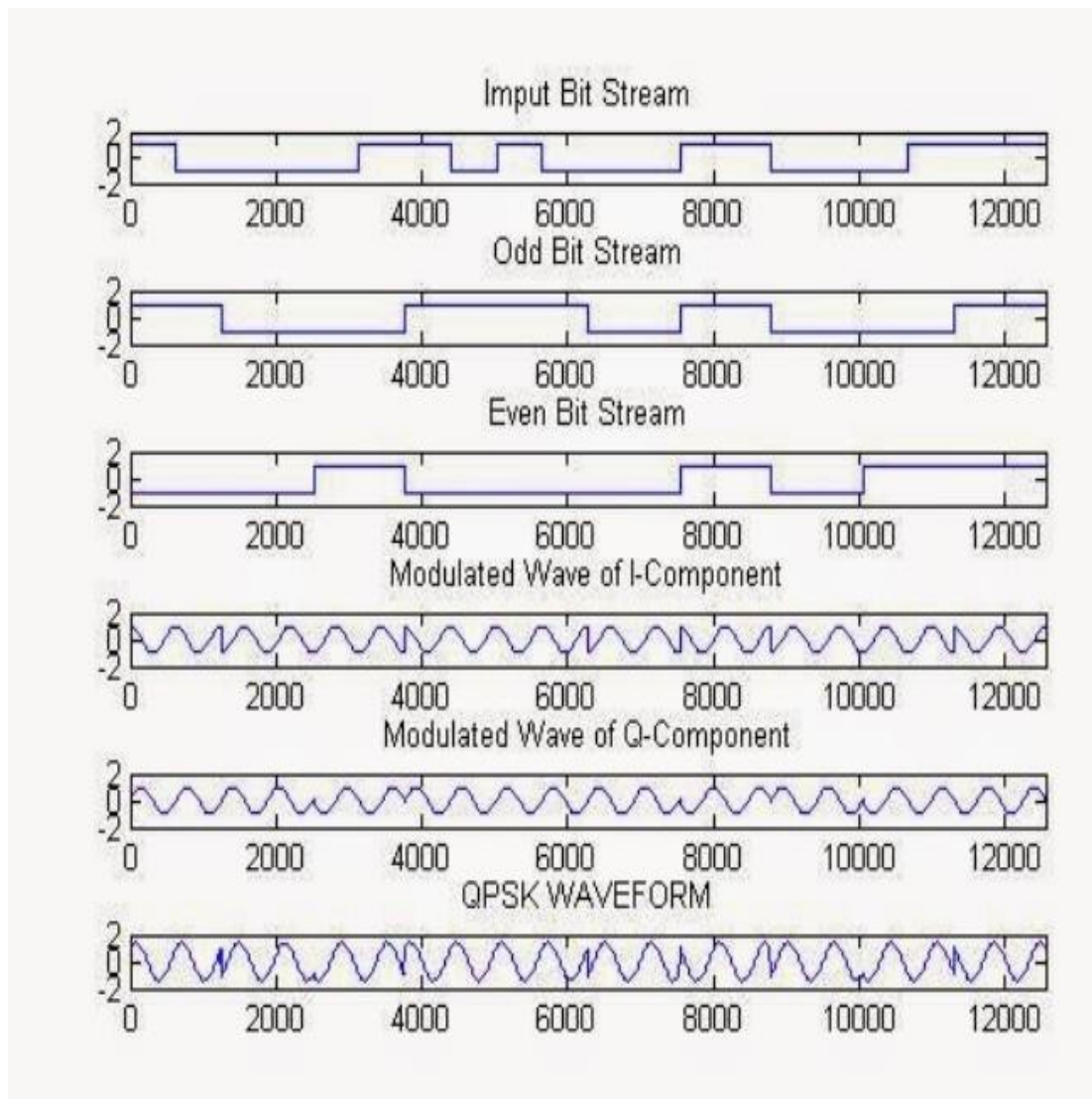
### Demodulation:

11. Apply the QPSK modulated output to the demodulator input.

12. Observe the multiplied signal of QPSK and carrier signal, cosine at TP-12 and also observe the multiplied signal of QPSK and carrier signal, sine at TP-13.

13. Observe the integrated output at I-channel (TP-14) and Q-channel (TP-15)

Input Bits	Phase of QPSK signal	Co-ordinates of message signal	
		S1	S2
10	$\pi/4$		
00	$3\pi/4$		
01	$5\pi/4$		
11	$7\pi/4$		

**EXPECTED WAVE FORMS:****RESULT:**

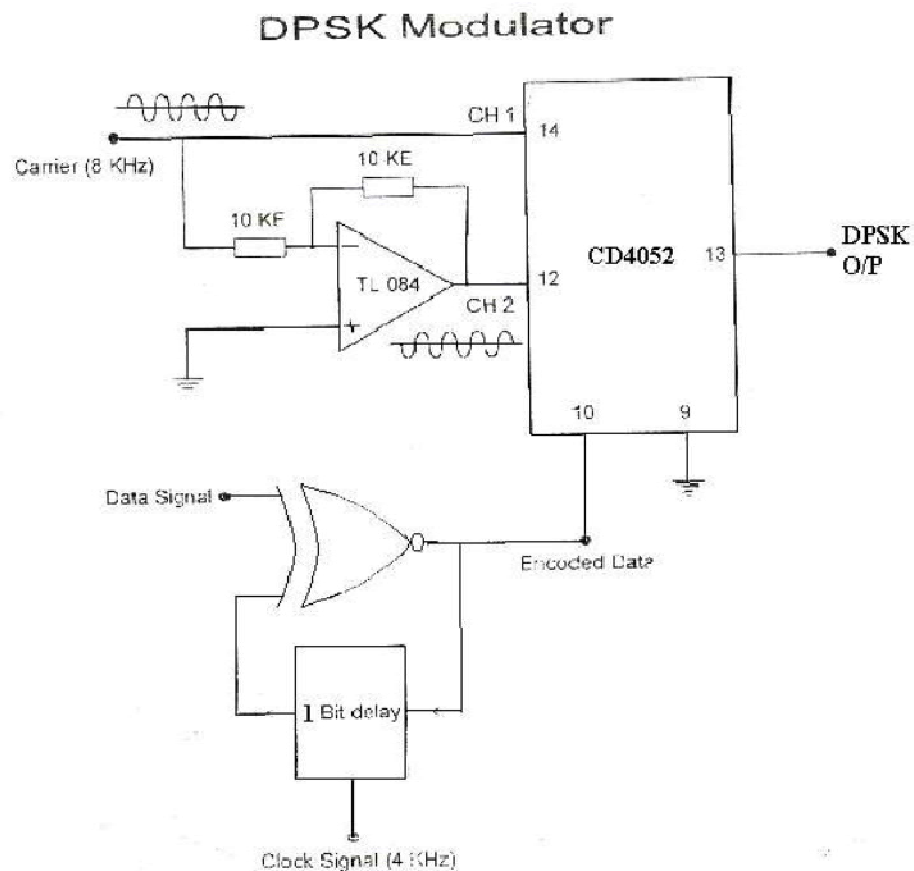
## DIFFERENTIAL PHASE SHIFT KEYING

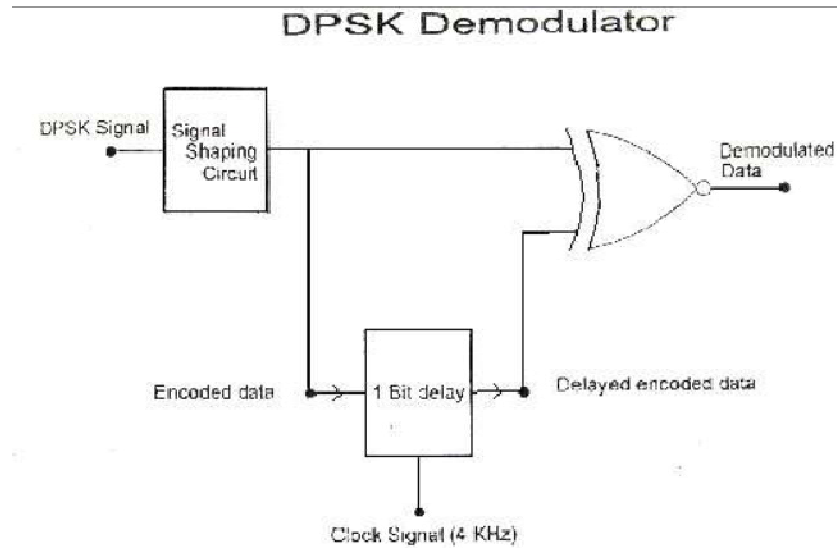
**AIM:** Study the characteristics of differential phase shift keying

### APPARATUS:

1. DPSK Trainer Kit
2. Dual Trace oscilloscope
3. Digital Multimeter
4. C.R.O(30MHz)
5. Patch chords.
6. PC with windows(95/98/XP/NT/2000)
7. MATLAB Software with communication toolbox

### BLOCK DIAGRAM:





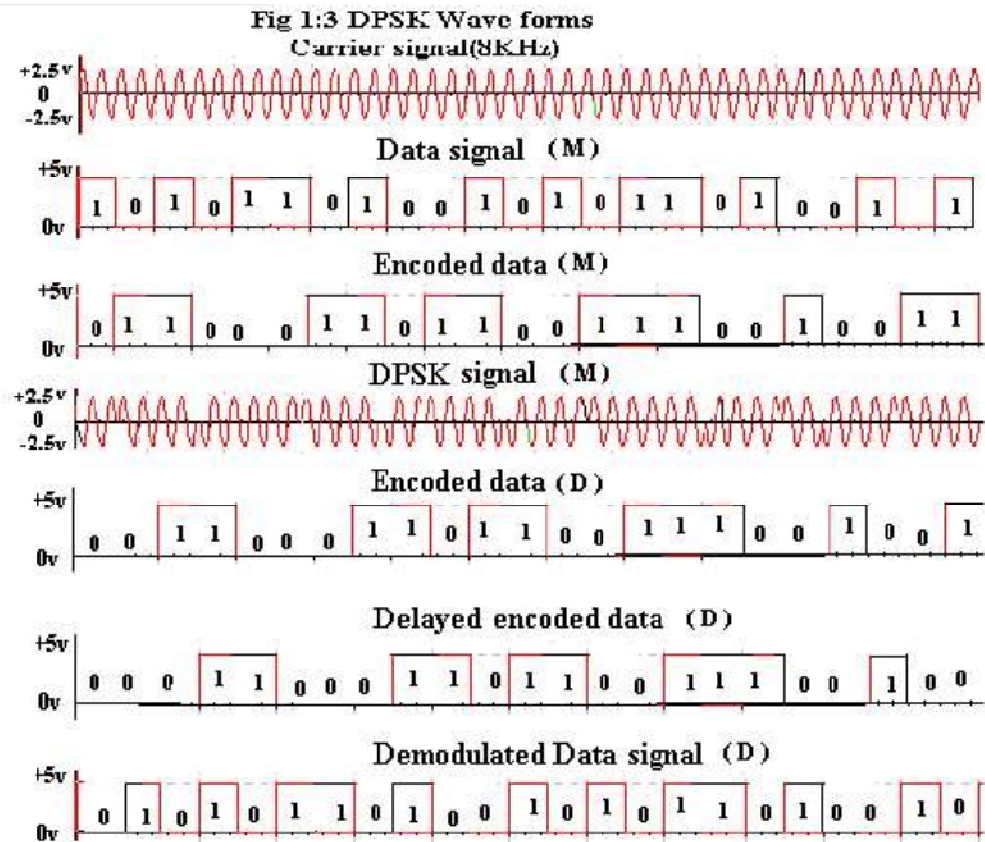
### **PROCEDURE: MODULATOR**

1. Connect carrier signal to carrier input of the PSK Modulator.
2. Connect data signal from data input of the X-NOR gate.
3. Keep CRO in dual mode.
4. Connect CH1 input of the CRO to data signal and CH2 input to the encoded data (which is nothing but the output of the X-NOR gate)
5. Observe the encoded data with respect to data input. The encoded data will be in a given sequence.
6. Actual data signal : 10101101001010110100
7. Encoded data signal : 01100011011001110010
8. Now connect CH2 input of the CRO to the DPSK output and CH1 input to the encoded data. Observe the input and output waveforms and plot the same.
9. Compare the plotted waveforms with the given waveforms in fig: 1.3
10. Note: Observe and plot the waveforms after perfect triggering. Better to keep the encoded data more than 4 cycles for perfect triggering.

## DEMODULATOR

1. Connect DPSK signal to the input of the signal shaping circuit from DPSK transmitter with the help of coaxial cable (supplied with trainer).
2. Connect clock from the transmitter (i.e. DPSK Modulator) to clock input of the 1 bit delay circuit using coaxial cable.
3. Keep CRO in dual mode. Connect CH1 input to the encoded data (at modulator) and CH2 input to the encoded data (at demodulator).
4. Observe and plot both the waveforms and compare it with the given waveforms. You will notice that both the signals are same with one bit delay.
5. Keep CRO in dual mode. Connect CH1 input to the data signal (at modulator) and CH2 input to the output of the demodulator.
6. Observe and plot both the waveforms and compare it with the given waveforms. You will notice that both the signals are same with one bit delay.

Disconnect clock from transmitter and connect to local oscillator clock (i.e., clock generator output from De Modulator) with remaining setup as it is. Observe demodulator output and compare it with the previous output. This signal is little bit distorted. This is because lack of synchronization between clock at modulator and clock at demodulator. You can get further perfection in output waveform by adjusting the locally generated clock frequency by varying potentiometer.

**EXPECTED WAVEFORMS:**

**DC LAB**  
**PART – B (SOFTWARE)**

**SOFTWARE EXPERIMENTS (PART-B)**  
**Modeling of Digital Communications using MATLAB**

1. Study Sampling Theorem and verify the effect of under sampling and over sampling while retrieving the original signal.
2. Understand functioning of each block in Pulse code modulation circuit and verify through simulation.
3. Write a program on Differential pulse code modulation and demodulation.
4. Write a program on Frequency shift keying modulation schemes for given two carrier frequencies, determine the bit error probability.
5. Write a program and verify QPSK modulation and demodulation, determine the bit error probability.
6. Write a program and verify Differential phase shift keying modulation scheme is a non-coherent modulation scheme, determine the bit error probability is inferior to that of QPSK.

SVR ECE



## 1.SAMPLING THEOREM

**Aim:** To verify the Sampling Theorem using MATLAB Software

### **Apparatus Required:**

1. PC with 64 bit OS
2. Matlab Software 2016a

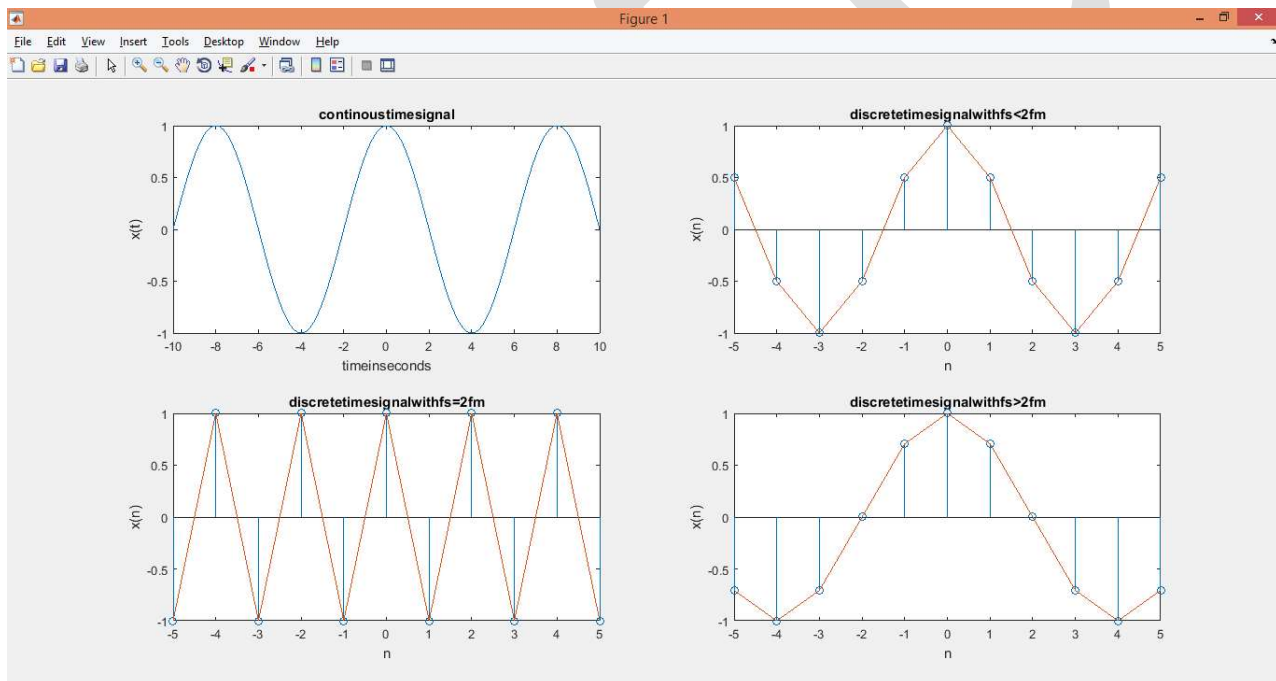
### **PROGRAM FOR SAMPLING THEOREM:**

```

clc
close all;
clear all;
t=-10:0.01:10;
T=8;
fm=1/T;
x=cos(2*pi*fm*t); fs1=1.2*fm; fs2=2*fm; fs3=8*fm;
n1=-5:1:5;
xn1=cos(2*pi*n1*fm/fs1); subplot(221)
plot(t,x);
xlabel('timeinseconds'); ylabel('x(t)');
title('continuous timesignal'); subplot(222)
stem(n1,xn1); hold on;
plot(n1,xn1);
xlabel('n');
ylabel('x(n)');
title('discretetimesignalwithfs<2fm');
n2=-5:1:5;
xn2=cos(2*pi*n2*fm/fs2); subplot(223)
stem(n2,xn2);
holdon;
plot(n2,xn2)
xlabel('n');
ylabel('x(n)');
title('discretetimesignalwithfs=2fm');

```

```
n3=-5:1:5;  
xn3=cos(2*pi*n3*fm/fs3);  
subplot(2,2,4)  
stem(n3,xn3);  
hold on;  
plot(n3,xn3);  
xlabel('n');  
ylabel('x(n)');  
title('discretetimesignalwithfs>2fm')
```



**Result:** Successfully verified Sampling Theorem using MATLAB Software.

## 2.PULSE CODE MODULATION & DEMODULATION

**Aim:** To generate a Pulse Code Modulated Signal using MATLAB software

### **Apparatus Required:**

1. PC with 64 bit OS
2. Matlab Software 2016a

### **PROGRAM FOR PULSECODE MODULATION & DEMODULATION:**

```
clc;
closeall;
clearall;
n=input('enter n for n-bit pcm: ');
n1=input('enetr no. of smaples in T: ');
l=2^n
x=0:2*pi/n1:4*pi;
s=8*sin(x);
subplot(3,1,1);
plot(s);
title('analog');
xlabel('t-->');
ylabel('amp-->');
subplot(3,1,2);
stem(s);
gridon;
title('smapled');
xlabel('t-->');
ylabel('amp-->');
vmax=8;
vmin=-vmax;
del=(vmax-vmin)/1;
part=vmin:del:vmax;
code=vmin-(del/2):del:vmax+(del/2);
```

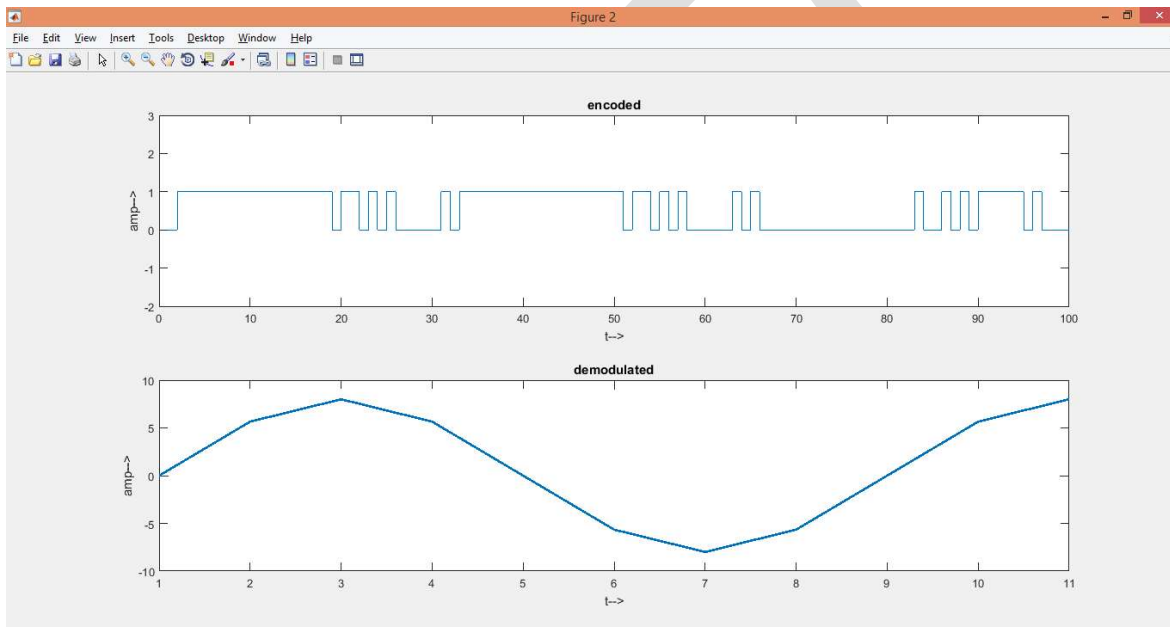
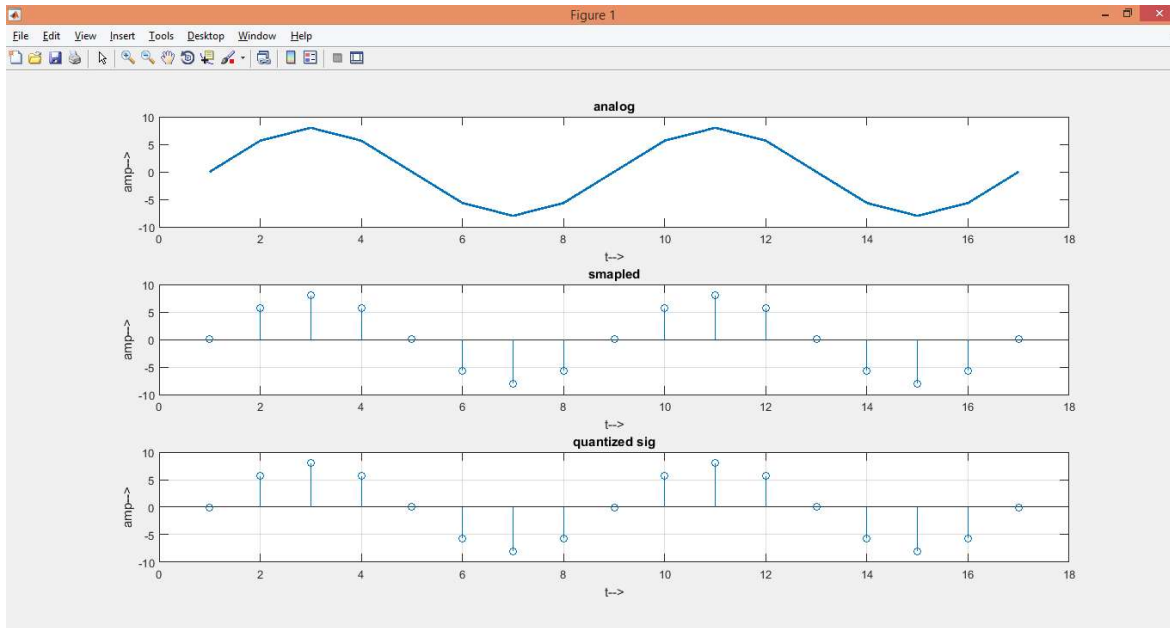
```
[ind,q]=quantiz(s,part,code);  
l1=length(ind);  
l2=length(q);  
for i=1:l1  
if(ind(i)~=0)  
ind(i)=ind(i)-1;  
end  
i=i+1;  
end  
for i=1:l2  
if(q(i)==vmin-(del/2));  
q(i)=vmin+(del/2);  
end  
end  
subplot(3,1,3);  
stem(q);grid on;  
title('quantized sig');  
xlabel('t-->');  
ylabel('amp-->');  
figure  
code=de2bi(ind,'left-msb');  
k=1;  
for i=1:l1  
for j=1:n  
coded(k)=code(i,j);  
j=j+1;  
k=k+1;  
end  
i=i+1;  
end  
subplot(2,1,1);  
grid on;  
stairs(coded);
```

```
axis([0 100 -2 3]);  
title('encoded');  
xlabel('t-->');  
ylabel('amp-->');  
  
qunt=reshape(coded,n,length(coded)/n);  
index=bi2de(qunt,'left-msb');  
  
q=del*index+vmin+(del/2);  
subplot(2,1,2);  
grid on;  
plot(q);  
title('demodulated');  
xlabel('t-->');  
ylabel('amp-->');
```

**INPUT:**

enter n for n-bit pcm: 16

enetr no. of smaples in T: 8



### 3.DIFFERENTIAL PULSE CODE MODULATION

**Aim:** To generate a Differential Pulse Code Modulated Signal using MATLAB software

#### **Apparatus Required:**

1. PC with 64 bit OS
2. Matlab Software 2016a

#### **PROGRAM FOR DIFFERENTIAL PULSECODE MODULATION :**

```
clc;
clearall;
closeall;
fid=fopen('speech_dft.mp3','r');
[m,count]=fread(fid,'int16');
count=8500;
fs=8000;
ts=1;
no_samples=(2*fs)+ts;
time=[1:fs/64];
mp=max(m);
bits=5;
levels=2^bits;
bit_rate=8000*bits;
alpha=0.45;
diff_sig(1)=m(1);
for k=2:count,
diff_sig(k)=m(k)-alpha*m(k-1);
end
dp=max(diff_sig);
stepsize=(2*mp)/levels;
for k=1:no_samples,
samp_in(k)=m(k*ts);
quant_in(k)=samp_in(k)/stepsize;
error(k)=(samp_in(k)-quant_in(k))/no_samples;
end
```

```
signs=sign(m);
quant_out=quant_in;
for i=1:count,
s(i)=abs(quant_in(i))+0.5;
quant_out(i)=signs(i)*round(s(i))*stepsize;
end
s_out=quant_out;
s_out(1)=quant_out(1);
for k=2:count,
s_out(k)=quant_out(k)+alpha*s_out(k-1);
end
nq=((stepsize)^2)/12*((mp/dp)^2);
snr=1.5*(levels^2);
snr_db=10*log10(snr);
subplot(4,1,1);
plot(time,m(time),time,s_out(time),'r');
title('input speech signal');
xlabel('time');
ylabel('m(t)');
grid on;
subplot(4,1,2);
plot(time,quant_in(time),'r');
title('quantized speech signal');
xlabel('time');
ylabel('levels');
grid on;
subplot(4,1,3);
plot(time,s_out(time));
title('decoded dpcm speech signal');
xlabel('time');
ylabel('dq(t)');
grid on;
subplot(4,1,4);
```



```
plot(time,error(time));  
title('error signal');  
xlabel('time');  
ylabel('error(t)');  
gridon;
```

## OUTPUT:

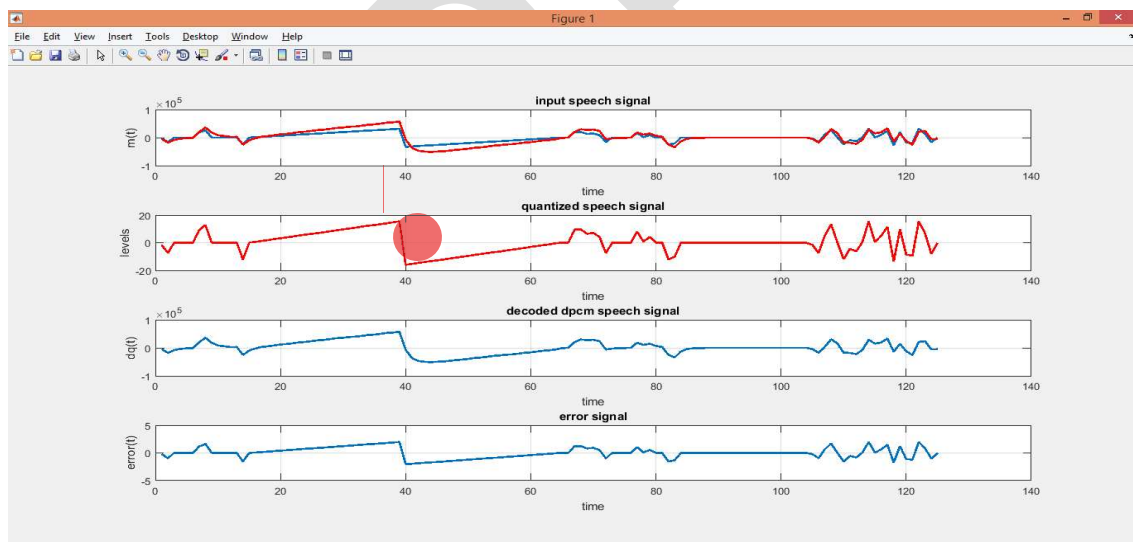
dp =46823

step size =2.0479e+03

nq = 1.7116e+05

snr =1536

snr\_db =31.8639



## 4. FREQUENCY SHIFT KEYING

**Aim:** To generate a FREQUENCY SHIFT KEYING using MATLAB software

### **Apparatus Required:**

1. PC with 64 bit OS
2. Matlab Software 2016a

### **PROGRAM FOR FREQUENCY SHIFT KEYING:**

```
clc;
close all;
clear all;

fc1=input('enter freq of 1st sine wave carrier:');
fc2=input('enter freq of 2nd sine wave carrier:');
fp=input('enter freq of periodic binary pulse (message):');
amp=input('enter the amplitude for both message and carrier');
amp=amp/2;

t=0:.001:1;

c1=amp.*sin(2*pi*fc1*t);
c2=amp.*sin(2*pi*fc2*t);

subplot(4,1,1)
plot(t,c1)
xlabel('t');
ylabel('a');
title('carrier 1 wave');

subplot(4,1,2)
plot(t,c2)
xlabel('t');
ylabel('a');
title('carrier 2 wave');

m=amp.*square(2*pi*fp*t)+amp;

subplot(4,1,3)
plot(t,m)
xlabel('t');
ylabel('a');
```

```
title('binary message pulses');  
  
for i=0:1000  
    if m(i+1)==0  
        mm(i+1)=c2(i+1);  
    else  
        mm(i+1)=c1(i+1);  
    end  
end  
  
subplot(4,1,4)  
plot(t,mm)  
xlabel('t');  
ylabel('a');  
title('modulated wave');
```

**Input:**

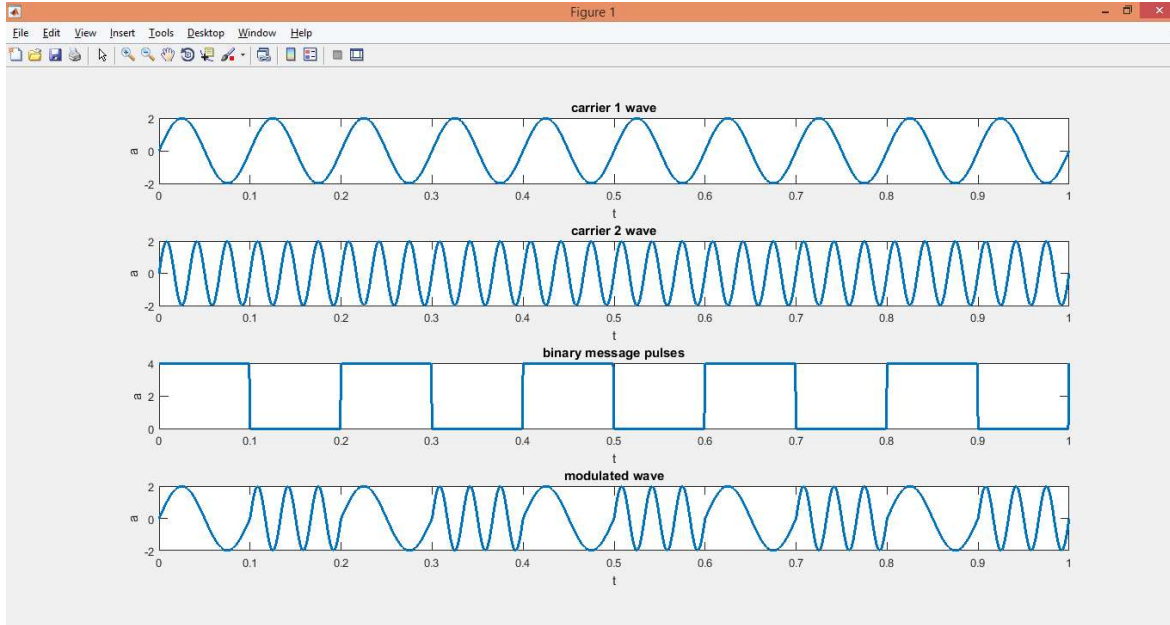
Enter freq of 1st sine wave carrier:10

Enter freq of 2nd sine wave carrier:30

Enter freq of periodic binary pulse (message):5

enter the amplitude for both message and carrier 4

### OUTPUT:



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## 5. PHASE SHIFT KEYING

**Aim:** To generate PHASE SHIFT KEYING using MATLAB software

### **Apparatus Required:**

1. PC with 64 bit OS
2. Matlab Software 2016a

### **PROGRAM FOR PHASE SHIFT KEYING:**

```
clc;

clearall;

closeall;

set(0, 'defaultlinewidth', 2);

A=5;

t=0:0.00001:0.01;

f1=input('CarrierSinewavefrequency=');

f2=input('Message frequency ='); x=A.*sin(2*pi*f1*t);%Carrier Sine

subplot(3,1,1);

plot(t,x);

xlabel('time');

ylabel('Amplitude');

title('Carrier');

gridon;

u=square(2*pi*f2*t);%Messagesignal

subplot(3,1,2);

plot(t,u);

xlabel('time');

ylabel('Amplitude'); title('MessageSignal');

gridon;

v=x.*u;%Sine wave multiplied with square wave

subplot(3,1,3);

plot(t,v);

axis([0 0.01 -6 6]);

xlabel('t');

ylabel('y');
```

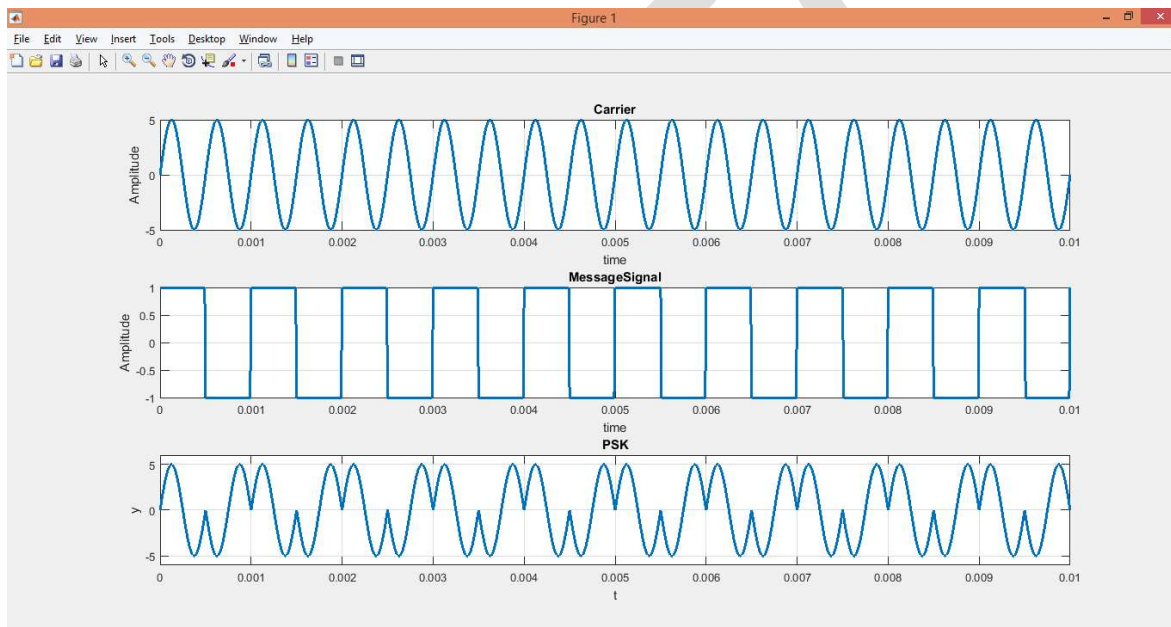
```
title('PSK');  
grid on;
```

## INPUT:

Carrier Sine wave frequency=2000

Message frequency =1000

## OUTPUT:



## 6. DIFFERENTIALPHASE SHIFT KEYING

**Aim:** To generate DIFFERENTIALPHASE SHIFT KEYING using MATLAB software

### **Apparatus Required:**

1. PC with 64 bit OS
2. Matlab Software 2016a

### **PROGRAM FOR DIFFERENTIAL PHASE SHIFT KEYING:**

```
clc;

clearall;

closeall;

n=100;

x=[ones(1,20) zeros(1,20) ones(1,20) zeros(1,20) ones(1,20)];

subplot(4,1,1);

plot(x);

title('input signal');

xlabel('number of samples');

ylabel('amplitude');

f=1*10^6;

fs=10*10^6;

for i=0:n-1

d(i+1)=sin(2*pi*(f/fs)*i);

end

subplot(4,1,2);

plot(d);

title('carrier signal');

xlabel('number of samples');

ylabel('amplitude');

for i=0:n-1

if(x(i+1)==0)

x(i+1)=sin(2*pi*(f/fs)*i);

else

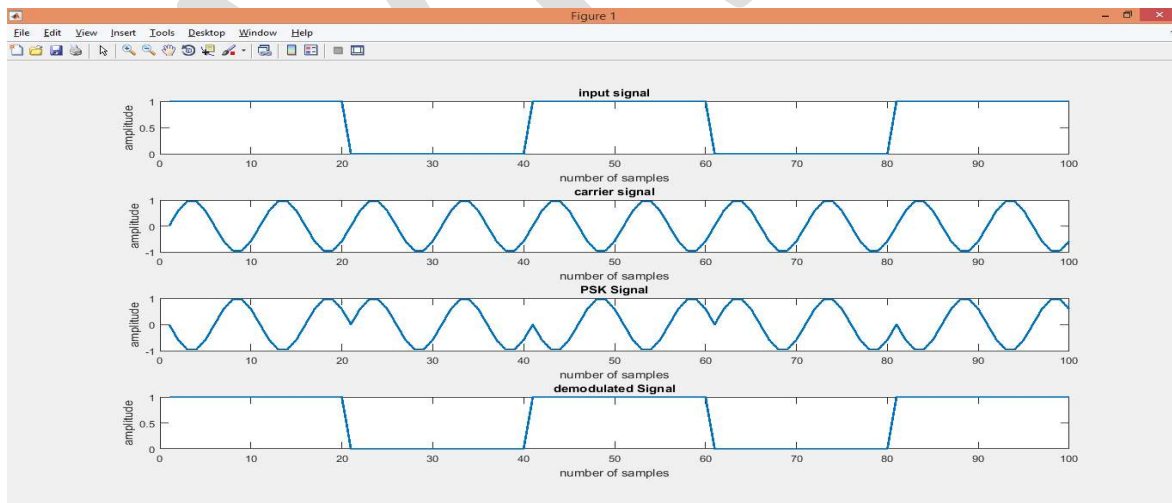
x(i+1)=sin(2*pi*(f/fs)*i+pi);

end

end
```

```
subplot(4,1,3);  
plot(x);  
title('PSK Signal');  
xlabel('number of samples');  
ylabel('amplitude');  
for i=0:n-1  
if(x(i+1)==sin(2*pi*(f/fs)*i))  
x(i+1)=0;  
else  
x(i+1)=1;  
end  
end  
subplot(4,1,4);  
plot(x);  
title('demodulated Signal');  
xlabel('number of samples');  
ylabel('amplitude');
```

### Output:



### RESULT:

Thus the DPSK modulation and demodulation were performed and graphs were plotted.



## QUADRATURE PHASE SHIFT KEYING

**Aim:** To generate QUADRATURE PHASE SHIFT KEYING using MATLAB software

### **Apparatus Required:**

1. PC with 64 bit OS
2. Matlab Software 2016a

clc;

clearall;

closeall;

t=0:0.1:4;

cvx=input('Enter Length of Random Bit Sequence:');

d=round(rand(1,cvx));

l=cvx;

x=0:0.01:1\*2\*pi;

cc=cos(x);

cs=cos(x+pi/2);

k=length(cc);

k1=k/l;

fori=1:l

if(d(i)==0)

d(i)=-1;

i=i+1;

end

end

i=1;

j=1;% To segregate odd bit streams and even bit streams

while (i<l) && (j<l) %half stream with double symbol duration

dd1(j)=d(i);

dd1(j+1)=d(i);

dd2(j)=d(i+1);

dd2(j+1)=d(i+1);

```
j=j+2;
i=i+2;
end% to make bit streams cycle equivalent to sinusoidal waveform
t=1;
for i=1:l
for j=1:k1 %k1 sample with 1 sine period
dd(t)=d(i);
d1(t)=dd1(i);
d2(t)=dd2(i);
t=t+1;
j=j+1;
end
i=i+1;
end

subplot(6,1,1);
stairs(dd);
axis([0 t -2 2]);
title('Imput Bit Stream');
subplot(6,1,2);
stairs(d1);
axis([0 t -2 2]);
title('Odd Bit Stream');
subplot(6,1,3);
stairs(d2);
axis([0 t -2 2]);
title('Even Bit Stream');

len=length(d1);
if(k<len)
len=k;
end
```

```
for i=1:len
qcc(i)=cc(i)*d1(i);% odd streams multiplied with I waveform
qcs(i)=cs(i)*d2(i);% even streams multiplied with Q waveform
i=i+1;
end
```

```
subplot(6,1,4);
plot(qcc);
axis([0 len -2 2]);
title('Modulated Wave of I-Component');
subplot(6,1,5);
plot(qcs);
axis([0 len -2 2]);
title('Modulated Wave of Q-Component');
```

```
qp=qcc+qcs; % QPSK output from Adder
subplot(6,1,6);
plot(qp);
axis([0 len -2 2]);
title('QPSK WAVEFORM');
figure, scatter(dd1,dd2,40,'*r');
title('Constellation Diagram of QPSK');
```

## QUADRATURE PHASE SHIFT KEYING

**Aim:** To study the Modulation and Demodulation Techniques of QPSK

### Apparatus Required:

1. PC with 64 bit OS
2. Matlab Software 2016a

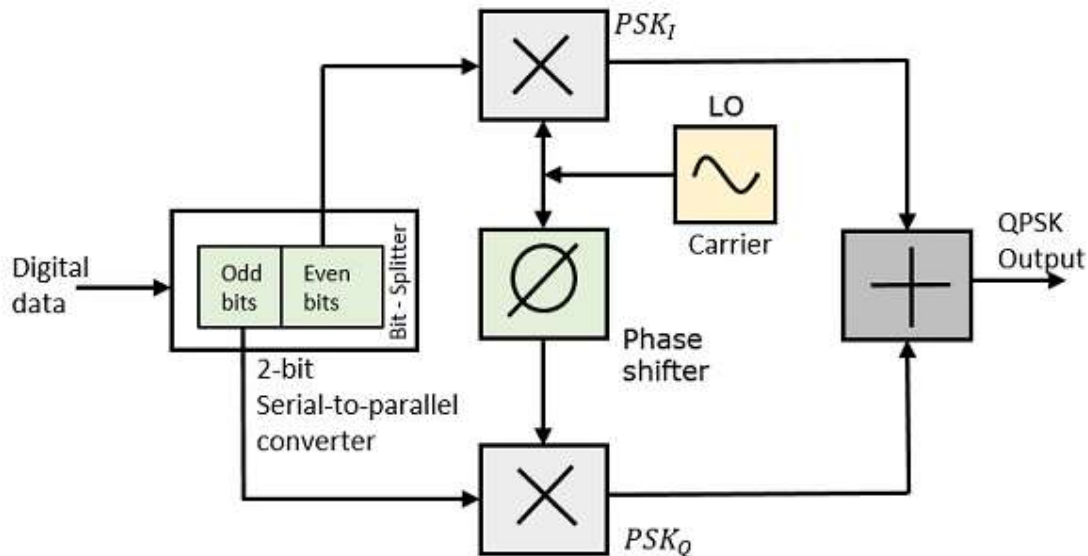
### **THEORY:**

The **Quadrature Phase Shift Keying** is a variation of BPSK, and it is also a Double Side Band Suppressed Carrier DSBSC modulation scheme, which sends two bits of digital information at a time, called as **bigits**.

Instead of the conversion of digital bits into a series of digital stream, it converts them into bit pairs. This decreases the data bit rate to half, which allows space for the other users.

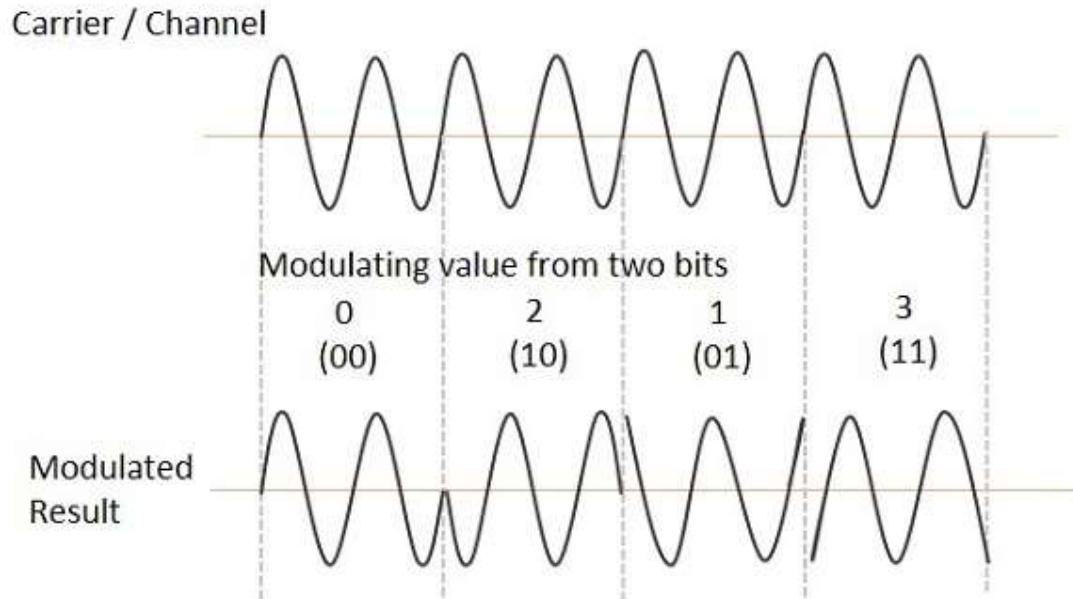
### **QPSK Modulator**

The QPSK Modulator uses a bit-splitter, two multipliers with local oscillator, a 2-bit serial to parallel converter, and a summer circuit. Following is the block diagram for the same.



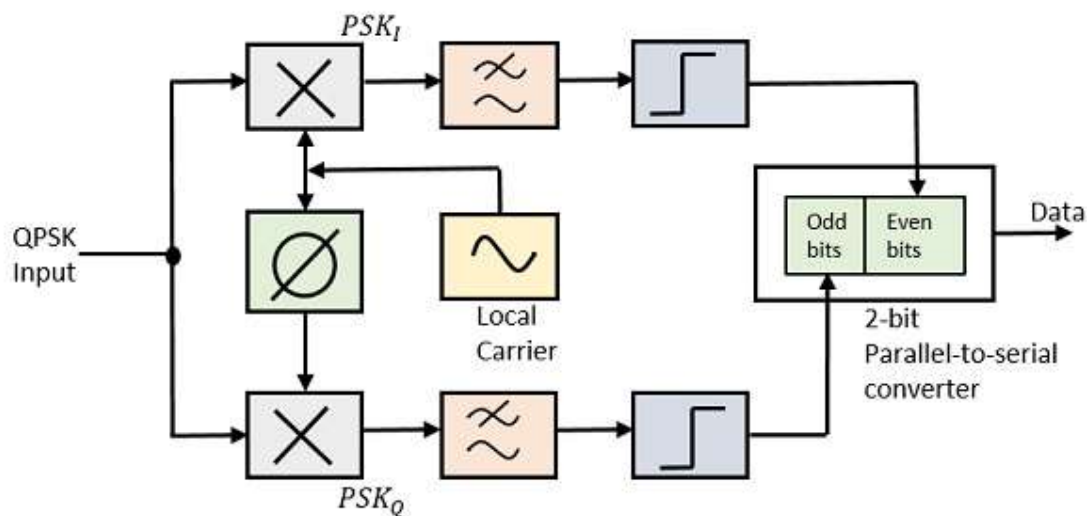
At the modulator's input, the message signal's even bits (i.e., 2<sup>nd</sup> bit, 4<sup>th</sup> bit, 6<sup>th</sup> bit, etc.) and odd bits (i.e., 1<sup>st</sup> bit, 3<sup>rd</sup> bit, 5<sup>th</sup> bit, etc.) are separated by the bits splitter and are multiplied with the same carrier to generate odd BPSK (called as  $PSK_I$ ) and even BPSK (called as  $PSK_Q$ ). The  $PSK_Q$  signal is anyhow phase shifted by  $90^\circ$  before being modulated.

The QPSK waveform for two-bits input is as follows, which shows the modulated result for different instances of binary inputs.



## QPSK Demodulator

The QPSK Demodulator uses two product demodulator circuits with local oscillator, two band pass filters, two integrator circuits, and a 2-bit parallel to serial converter. Following is the diagram for the same.



The two product detectors at the input of demodulator simultaneously demodulate the two BPSK signals. The pair of bits are recovered here from the original data. These signals after processing, are passed to the parallel to serial converter.

**Program:**

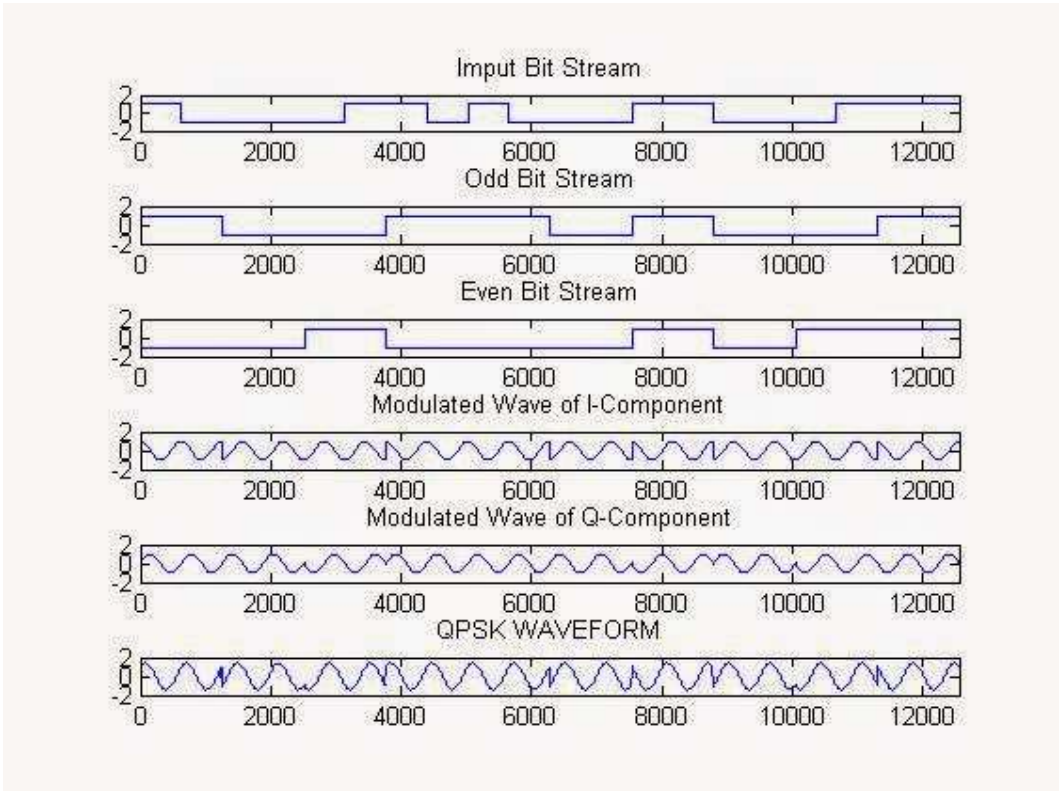
```

clc;
clearall;
closeall;
t=0:0.1:4;
cvx=input('Enter Length of Random Bit Sequence:');
d=round(rand(1,cvx));
l=cvx;
x=0:0.01:l*2*pi;
cc=cos(x);
cs=cos(x+pi/2);
k=length(cc);
k1=k/l;

for i=1:l
if(d(i)==0)
d(i)=-1;
i=i+1;
end
end
i=1;
j=1;% To segregate odd bit streams and even bit streams
while (i<l) && (j<l) %half stream with double symbol duration
dd1(j)=d(i);
dd1(j+1)=d(i);
dd2(j)=d(i+1);
dd2(j+1)=d(i+1);
j=j+2;
i=i+2;
end% to make bit streams cycle equivalent to sinusoidal waveform
t=1;
for i=1:l
for j=1:k1 %k1 sample with 1 sine period
dd(t)=d(i);
d1(t)=dd1(i);
d2(t)=dd2(i);
t=t+1;
j=j+1;
end
i=i+1;
end

subplot(6,1,1);
stairs(dd);
axis([0 t -2 2]);
title('Input Bit Stream');
subplot(6,1,2);
stairs(d1);
axis([0 t -2 2]);
title('Odd Bit Stream');
subplot(6,1,3);
stairs(d2);
axis([0 t -2 2]);
title('Even Bit Stream');

```



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**BEYOND THE SYLLUBUS**  
**EXPERIMENTS**

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## PSK MODULATION & DEMODULATION

**Aim:** To study the Modulation and Demodulation Techniques of PSK

### Equipment Required:

1. PSK Kit
2. Power Supply
3. 20MHz CRO
4. CRO Probes
5. Patch chords

**Theory:** In the PSK modulation or phase shift keying, for all the 'one' to 'zero' transitions of the modulating data, the modulated output switches between the in phase and out of phase components of the modulating frequency if the modulated carrier is represented by,

$$M(t) = A(t) \cos(\omega t + \text{phase})$$

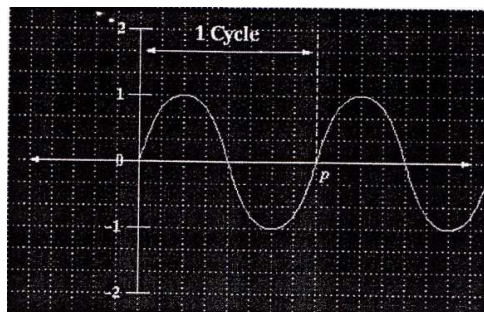
Where  $(t)$  = Time varying amplitude  
 $\omega t$  = Time varying angle  
 $(t)$  = Modulated carrier

PSK describes the modulation technique that alters the phase of the carrier. Mathematically,

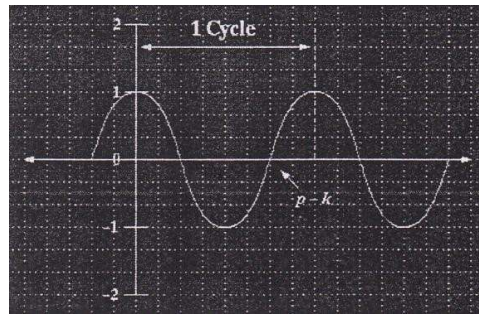
$$s(t) = \sin(2\pi f_c t + \phi(t))$$

1. In angle modulation, the phase of the carrier is discretely varied in relation either to a reference phase or to the phase of the immediately preceding signal element, in accordance with data being transmitted.
2. In a communication system, the representation of characters, such as bits or quaternary digits, is done by a shift in the phase of an electromagnetic carrier wave with respect to a reference, by an amount corresponding to the symbol being encoded. Note 1: For example, while encoding bits, the phase shift could be  $0^\circ$  for encoding a "0", and  $180^\circ$  for encoding a "1", or the phase shift could be  $-90^\circ$  for "0" and  $+90^\circ$  for a "1", thus making the representations for "0" and "1" a total of  $180^\circ$  apart. Note 2: PSK systems are designed so that the carrier can assume only two different phase angles, each change of phase carries one bit of information, i.e., the bit rate equals the modulation rate. If the number of recognizable phase angles is increased to 4, then 2 bits of information can be encoded into each signal element; likewise, 8 phase angles can encode 3 bits in each signal element.

Phase shift keying is a technique which shifts the period of a wave. This wave has a period of  $t$ , noted above. Also notice that the start of the wave's period is at 0.



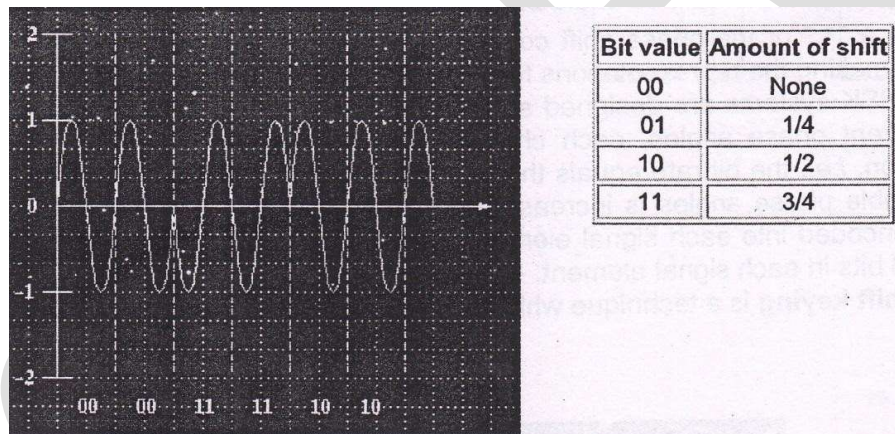
WAVE-1



## WAVE-2

Wave 2 is the same wave as the first, but its phase has been **shifted**. Notice that the period starts at the wave's highest point (1). So what's the point? Such a behavior is seen because we have shifted this wave by **one quarter** of the wave's full period. We can shift it to another quarter, if we want to, so the original wave would be shifted by **half** its period. And, we could do it one more time, so that it would be shifted **three quarters** of its original period.

This means that, we have 4 separate waves. So why not let each wave stand for some binary value? Since there are 4 waves, we can let each wave signify 2 bits (00, 01, 10, 11).



This technique of allowing each shift of a wave represent some bit value is **phase shift keying**. But, the real key is to shift each wave relative to the wave that came before it. An example can be seen in the above diagram.

Please note that when binary values were chosen randomly, for each wave, the values shown are incorrect. Thus, the correct pattern should be: 00 01 10 00 10 00.

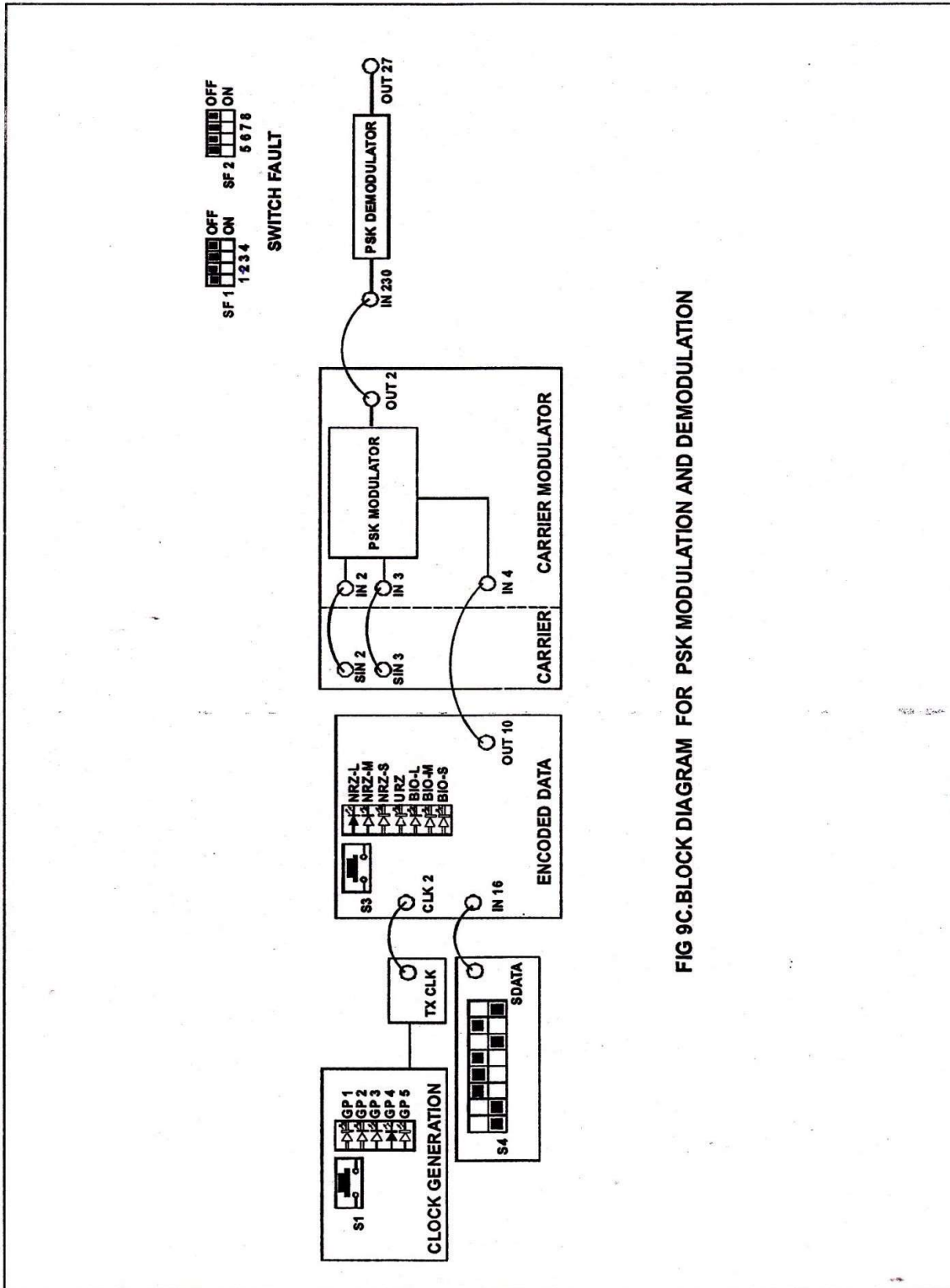


FIG 9C.BLOCK DIAGRAM FOR PSK MODULATION AND DEMODULATION

I/PSin1–

3.4Vpp,1.04MHzl/PSin2–

3.4Vpp,1.04MHz

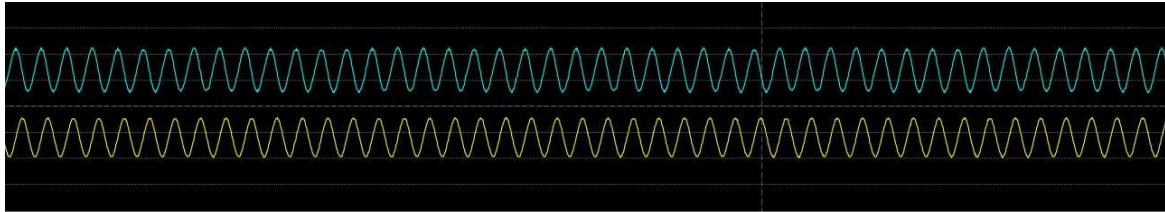


Figure1:InputSignals

Data1/P–9.4Vpp,33.1KHz

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Figure2: I/P Data &amp; Modulated O/P

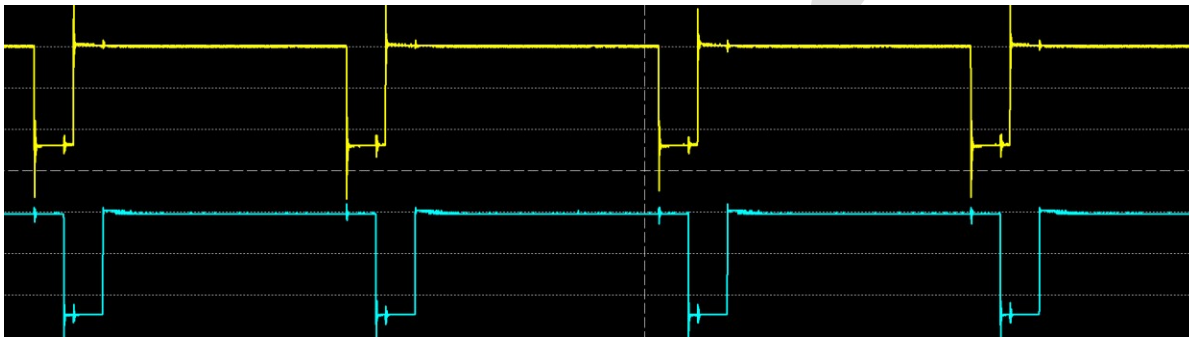


Figure3: I/P Data &amp; Recovered O/P

Fig: PHASE SHIFT KEYING MODULATION & DEMODULATION  
MODEL WAVEFORMS

#### Procedure for DCL-01 Kit:

- Ensure that the group **4 (GP4)** clock is selected in the Clock Generation section. Selection is done with the help of switch S1 and observes the corresponding LED indication.
- Observe the transmitter clock of frequency **250KHz** at **TXCLK** post.
- Set the data pattern using switch S4 as per the given block diagram.
- Observe the 8-bit data pattern at **SDATA** post.
- Observe the carrier sine waves of frequencies **1MHz** at **SIN2** post and **1MHz** with **180°** phase at **SIN3** post in the carrier section.

## DCS LABMANUAL

- Connect the **SIN2** post to the **IN2** post and **SIN3** post to the **IN3** post of the Carrier modulator section.
- Connect **S DATA** to **IN16** post and **TXCLK** to **CLK2** post of the Encoded Data section.
- Select **NRZ-L** data with the help of the switch **S3** and observe the corresponding LED indication in the Encoded Data section.
- Connect **OUT10** post of the Encoded Data section to **IN4** post as a control input for the carrier modulator section.
- Observe the **PSK** modulated signal at the **OUT2** post of the Carrier modulator section.
- For the demodulation of the **PSK** modulated data, connect the **OUT2** post of the carrier modulator to the **IN30** post of the PSK demodulator section.
- Observe the PSK demodulated data at **OUT27** post of the PSK demodulator section.
- Verify the recovered data with the **SDATA**.

## RESULT: